

# CADSTAR Express – Version 13.0



**Do-it-Yourself Training Booklet** 





# CADSTAR Express Do-It-Yourself Book With Projects For Educational Purpose

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#### Hello!

My name is 'DIY-booklet' and I'm glad to see you have picked me up. I am from **ZUKEN** and it is good to meet you. If you are wondering where this is, take a look at <u>www.zuken.com/cadstar</u>, my "home"-page.

With this booklet, you have received a free copy of CADSTAR Express. CADSTAR Express provides a number of features of the full CADSTAR version, only limited by the number of components (max 50) and pads (max 300).

To install CADSTAR Express, double click on the executable for set-up and simply follow the instructions.

If you are seriously thinking about designing a Schematic and Printed Circuit Board (PCB), you have made the right decision to come to me. You will find out in detail how you can make use of CADSTAR to design a Schematic and PCB. I will start by showing you a hand drawn electronic circuit and transforming this to a professional schematic design. Then I'll take you through the process of creating an error-free transfer of data to a PCB, and then move to layout and routing. The second step I will show you is how to create and add a component to your library.

Spend some time with me and you will learn a lot in a short time.



It is not difficult to capture a schematic and to design a PCB, but if I was not clear enough, just click on the camera icon every time you come across it, and watch me (you will need an internet connection for this)!



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  - Step 1 Insert Reuse Block
- Conclusion

Please Note: This do-it-yourself guide has been revised using a Windows 7 environment. The software has been installed on the author's computer using the default locations and selections per the CADSTAR Express rev 13 SETUP program. If you are using Windows XP your default path and file locations will differ from the images displayed in this guide.



#### • Introduction to CADSTAR

Let me introduce CADSTAR to you. CADSTAR is an EDA design tool allowing you to draw a schematic design and transfer the design to a PCB layout environment. After an error-free transfer, CADSTAR helps to place the components into the board outline.

Placement and Routing is an integral part of a PCB design process. CADSTAR offers much flexibility in this area by providing both Push-a-side Placement and Routing tools (manual, semi-automatic and fully automatic) within the Embedded Place & Route Editor or the advanced standalone Place & Route Editor. The Embedded Place & Route Editor has been developed in general for basic PCB design or users who don't use a PCB design tool regularly, and the standalone Place & Route Editor is for the more advanced users who require more powerful functions. For really advanced users (industry users) high-speed design features (such as lengthening, delay, impedance, cross-talk, overshoot, reflection etc.) can also be provided in a full standard package or as an optional add-on. The additional add-on's that are available to you, include BoardModeler Lite which is a *unique* 3D verification tool for PCB design that provides a complete new concept of PCB Design in a 3D environment or the CADSTAR Variant Manager which enables you to generate variants of a 'master' design (included B.O.M's and assembly drawings) without having to maintain separate files for each variant.

The completion of the PCB design will be followed by the generation of manufacturing output data for PCB fabrication.

I will guide you through the basic design flow of a PCB design and through some very simple PCB designs using CADSTAR. *Try them and have fun!* 





#### • Let's Get Started!

By now you have probably installed CADSTAR on your PC and are anxious to get started. Start by clicking the **Design Editor** Icon in your **Start**-**Programs**-**CADSTAR Express** menu. When CADSTAR is started you will see the **Start page** as shown below.

	Start Page - Zuken CADSTAR Design Editor Express _				
Eile View Libraries Tools Windo	w Help				
	🗠 1, 📰 🌒 (DEFAULT) 💽 📙 🛄 📮				
Copen Designs V A X					
Current Design	CADSTAR Express Design Edi Recent Workspace Files  Cent Design Files  Copen Workspace Save New Workspace  Recent Design Files  Copen File New File  Open File New File  Coting Started Copen File New File  Coting Started Copen File New File  Coting Started Copen File New File  Copen	<text><section-header><section-header><section-header><form><image/><text><text><text><text><text><text><text><text><text></text></text></text></text></text></text></text></text></text></form></section-header></section-header></section-header></text>			
Bus Report E Design Rule	Fronts Rel Electrical Rules Check R Overlanning Connections R Routing Completion	Unused Components	V		
E bus keport E Design Kule	Chors Check Check P Overlapping connections C Routing Completion	onuscu components			

This page serves as a Concierge. It allows you to;

- Access recently opened Workspace Files
- Access recently opened Designs,
- Access Help and PDF files
- Read up on the latest in CADSTAR News from the World of Zuken.
- Access some or On-line Links such as the On-Line Library and our CADSTAR Web pages.

CADSTAR is a Multi-Document Design Environment. Soon you will have schematic designs and PCB designs all open in the same *Design Editor* environment.



#### • The Basic Design Flow

Library Usually you need to start off with a library and to ensure that all the parts (schematic symbols & PCB footprints) that you will require are available to you. However, to complete the exercises in this DIY booklet you don't need to worry about the library. Nevertheless if you are keen on learning more about the CADSTAR library you can try Chapter 3.

**Note:** the library provided with CADSTAR Express contains all the parts essential for the PCB designs described in this 'Do-It-Yourself Book' and some examples of the online CADSTAR Libraries. CADSTAR has made their evaluation software, CADSTAR EXPRESS, even more user friendly by adding a free download of a 20.000 Parts Library at our <u>website</u>. Additional libraries are available through the **Zuken on-line support website**. The ready-to-download-and-use parts contain all the information you require including manufacturers' part numbers. They are updated and expanded regularly with over **250,000 parts** currently available. If the part required is not available in these libraries, you can quickly and easily design your own parts using the supplied wizards and the Graphical Library Editor.

Access to the on-line CADSTAR Libraries is available as part of annual maintenance contracts.

**Schematic** It is always advisable to start with a schematic design before moving onto the PCB design (although CADSTAR does support reverse engineering).

**PCB** After the successful transfer from schematic, components will be placed within the **(Placement)** board outline.

**PCB** After placing all the components, we can start routing the critical nets manually and/or through automatic routing.

Manufacturing Output The final stage of any PCB design. No matter what your manufacturer requires, CADSTAR can deliver; extended Gerber (RS274X), extended N.C. Drill (Excellon), Placement data, Bill of Materials, IPC356-D test data, DXF and ODB++



#### • The User Interface

CADSTAR is very Easy to use! The User Interface is very consistent in operations whether you are editing a Schematic or a PCB Design.

CADSTAR Supports;

- Dockable Tool bars can be dragged and docked as needed.
- Tool bar Icons that can be allocated as the user wishes.
- Customizable Tool bars and Menus are supported for adding user defined reports and Macros.
- Tabbed Document Window support Most often seen in more modern version of Windows 7 and MS Office  $\ensuremath{\mathbb{B}}$
- "Strokes" command macros that perform the most common functions for panning and zooming.
- Themes to alter the appearance of CADSTAR when working in a more modern operating system, "Windows 7", such as Collapsible Menus for a more condensed menu appearance.
- Dockable Active reports Active reports can be placed anywhere just like any other dockable window in CADSTAR. The reports you currently have open will appear as tabs in the Active Report window.



# Strokes in CADSTAR and the Place & Route Editor

If you are not familiar with Stroke commands, you can use them for;

Indicating operations you wish the application to perform by dragging the right mouse button in the shape of one of the 'gestures' in the table below.

To make the gesture:

- Use the mouse to position the cursor in the design window
- Click the right mouse button and Hold while moving the mouse so that the cursor follows the path of the gesture. The application will provide feedback by drawing a white line showing the path of the cursor
- Release the right mouse button

**Note:** The shape of the path followed by the cursor is important. The direction which the cursor takes along the path is also important, since it is often true that each of the two different directions is associated with a different operation.

Gesture	Icon	Operation	Gesture	Icon	Operation
Î		Pan up	<b>~</b>	I	Pan left
	Ţ	Pan down			Pan right
	Æ	Zoom in		ସ	Zoom out
		View all (Display all of the drawing/design or component/symbol)		Q	Zoom to selected area (the minimum box which contains both the start and end points)
	đ	Redisplay the current view, repairing any damage to the objects displayed	Z	Q	Zoom to selected area [see above]
	ଷ୍	Previous View Revert to the view as it was before the last view-changing command such as pan or zoom			



# • Chapter 1 – Design A

#### Introduction to the LED Flasher

This is an A-stable multi-vibrator circuit to alternately flash two LEDs. The Resistor and the Capacitor values determine the frequency, which is the flash rate. The formula is as follows:





[Time Off =  $0.7 \times R \times C$ ] R in ohms and C in farads [Total Time Off = 1 / Frequency] Total Time Off being the total number of seconds that both transistors are off and Frequency is in hertz. [Time Half = Total Time Off / 2] [Capacitor = Time Half / (0.7 \* R)] with Capacitor answer in farads.

The design drawn has two 39 k Ohm resistors and 10uF capacitors. However, the two sides do not have to match. Different values for R and C on each side can give a nice effect for a unique duty-cycle. The flash-rate for this circuit is about one cycle per second.

The 470 Ohm collector load resistor limits the current flow to ~20mA and also determines the brightness of the LEDs. 270 or 330 Ohm is recommended for green LEDs. The transistors in this design are not critical.



#### Step 1 - Schematic for Design A

- a. Let's start with going through the hand drawn schematic shown previously the design of a simple LED flasher.
- b. You will then have to gather the components being used in the flasher.
- c. From the hand-drawn schematic, you should be able to find twelve (12) parts in the Library. They are;

Qty. per part

- 2 2N3904 NPN Transistor
- 2 1N914 Diode
- 2 LED HLMP-1585
- 2 470 Ohm Resistor
- 2 39k Ohm Resistor
- 2 10uF/10V Electrolytic Capacitor
- d. You can use a 9V battery for this power supply.
- e. Once this information is available, you can start within the CADSTAR Design Editor
- f. Click the <sup>□</sup> icon on the toolbar or select (**File→New Schematic Design**) and choose one of the templates in the box. (I like Form A4-euro)

Ne	w						×
	Schematic Design	PCB Design	Schematic Symb	ool   PCB Compor	nent 🗍 Documentatio	on Symbol	_
	Defaults	Form A1	Form A2	Form A3-EURO	Form A4-EURO		
						A3-euro -Size Sheet	
	Form B1	Form B2	Form C1	Form C2	Form D1		
	Form D2	Form E1	Form E2				
	Template Folder: C:\Users\Public\2	Zuken\CADSTA	R Express 13.0\	Templates		View New Design Settings	
					OK	Cancel Help	

g. When you select your template you can enter some information using the *Attributes* that have been created for you. These will appear in the Title block of the Schematic format. Later you can easily customize your own attributes and format sheets.



ew SCM Design		×			
Design Title					
A3-euro -Size Sheet					
Units Units: Thousa	ndths of an inch 💌 <u>N</u> umb	per of Decimal Places: 1			
Display grid	X Y Ster: 100.0	Grid lung: Reinte			
Colour Template Colour File : Attributes	(DEFAULT)				
Sheet Name	Doc Sym Reference/ Attribute Name	Doc Sym Position/			
Sheet1					
	FORMAT(A3-EURO)	(18000.0,1000.0)			
	Company name	JL Zuken			
	Drawn AB				
	Issued 09-09-15				
	Project name DIY				
	Project number xx-xxxxx-xx				
1	Revision	1			
		ÖK Cancel <u>H</u> elp			

**TIP:** If you don't like to work with a black background, you can also select from the toolbar, a different background colour scheme.

🧐 White Background SCM 🛛 🗸

You have just started a new schematic design, however your design is untitled, so why not select the **[File-)Save as...]** function and give it a real name.

You can now start calling out the symbols you require by using the Workspace on the left of the window.





**Note:** The Workspace tab menus for Libraries, Designs, Shape Properties, etc, can be automatically hidden if you wish. Simply Click the **Auto Hide** Icon shown above. When you move your cursor off of the workspace menu it will automatically slide to a hidden position. To show the menu again, drag your cursor back to the Workspace Tab on the left.

- i. Proceed to place two transistors onto the schematic
- Tip: For an advanced library search and filtering select Libraries→Library Searcher→Parts Library→Parts.lib (or any of the other Parts Libraries you want to search).
- j. Drag the transistor from the Workspace window, i.e. highlight 2N3904, click on it by using the left-hand mouse button, without releasing the button and drag it out onto the design template. Don't be frightened about the red markers on the pins as these are just zoom independent markers to highlight unconnected pins (the markers will disappear once you connect the pins).

ZUKEN



While dragging, you can use the right-hand mouse button <RMB> menu for mirror and/or rotation commands for the placement of a symbol. You can also use the 'm' or 'r' hotkeys before the component is placed or use a programmable function key like F3 to rotate. You can setup the function keys by selecting **Tools**->Customise->Keyboard.

**Tip:** For more information on hot key commands type '**?<enter>**' (this will appear on the command line at the lower left corner of the application).

	<b>.</b>	ibraries 耳	Shap	e Pro
		Bus Report	E	) D(
?				

k. Do the same for the other ten components (you can either select the through-hole or SMD components):

Qty. per part

- 2 Diode>1N914 (or BAS19)
- 2 Led>HLMP-1585
- 2 Resistor>470E-MRS25-1% (or 470E-r0805-2%)
- 2 Resistor>39K-MRS25-1% (or 39K-r0805-2%)
- 2 E-Capacitor>10uF-10V-EC (or 10uF-10V-c6032)



I placed mine like this.



You can move more than one component at a time. Hold down <Ctrl> button on the keyboard and make your selections and then Click and Drag them.



m. You can also use the Polygon and Freehand Selection functions to select everything within an area. Select the Tool bar icon and draw a polygon/fence around the items you want to select. When you are ready to select them simply Double Click the Left mouse button to accept the polygon or if using the freehand selection mode, just release the Left mouse button and then Click and Drag them.

An additional selection method is available in the *Tools*-*Options*-*[Interaction]* tab. Here you can choose between **Overlap** and **Cover** selection methods.

This gives more control over how items are selected during Frame Select, Polygon Select and Freehand Select.

- Use Cover to only select items completely covered by the selection shape.
- Use Overlap to select items partially covered by the selection shape.



A different cursor is displayed to show which selection method is in use. The selection method can be toggled by right clicking whilst drawing a selection shape. I.e. Holding down the Left Mouse Button and clicking the Right Mouse Button. Try it!

**TIP**: After adding the components into the design (like 2N3904), you can select the component and *click* on the right-hand mouse button to see a Link: On-line CADSTAR Datasheet. The link is a hyperlink to an URL on the internet (or intranet), but can also be linked to something different (i.e. PDF file or Word document). More links can be added to components in the CADSTAR Parts Library Editor. Be aware that some links might be out of date as the component has become obsolete.

Note: Parts can be allocated a special attribute value to control "Part Acceptance".

Parts Definitions						
Part Name	Number	Description	Version	Definition	SPICE	Part Acceptance
39K-MRS25-1%	2322-156-13903	Metal film resistor MRS25 39K 1%	2	39K-MRS25-1%		Obsolete - Replace with 39K-r0805-2%
39K-r0805-2%		Chip resistor 0805 39K 2%	2	39K-r0805-1%		
470E-MRS25-1%	2322-156-14701	Metal film resistor MRS25 470E 1%	1	470-MRS25-1%		
3E3-r0805-2%		Chip resistor 0805 3E3 2%	1	3E3-r0805-1%		
HLMP-1585	9322-018-62682	LED GREEN 3MM HLMP-1585	2	HLMP-1585		Only 10,000 pieces in Stock!
1N914		High-speed diode	1	1N914		
10uF-10V-c6032		10uF 10V Tantaal	1	10uF-10V-c6032		
SOLDEREYE-1MM	2413-015-02201	Soldereye 1.0 mm	2	SOLDEREYE-1MM		
Hole-2.0mm_Non-Plated		Hole 2.0 MM Non-Plated	2	Hole-2.0mm_Non-Plated		Not a Physical Part for Ordering
Hole-3.0mm_Non-Plated		Hole 3.0 MM Non-Plated	1	Hole-3.0mm_Non-Plated		

In the Parts Library image shown above, the column labeled "Part Acceptance" can hold a unique text reference to communicate a Part's Life cycle or inventory control measure to the user. This can be defined by the Librarian. When a part containing a Part Acceptance value is added to a Schematic design, the following warning dialog will be displayed.

Warning!	×				
	Part '39K-MRS25-1%' :- Obsolete - Replace with 39K-r0805-2%				
	Do you wish to continue?				
	<u>Y</u> es <u>N</u> o				





Accepting this Part will also store its value in the Design for later reflection in Parts List and various other report outputs.

	Part Details		
	Nam <u>e</u> :	39K-MRS25-1%	
	Number:	2322-156-13903	
The Drenest will be unfloated in the	Description:	Metal film resistor MRS25 39K 1%	
I he Property will be reflected in the Item Properties dialog	Library Path:	C:\Program Files\Zuken\CADSTAR Express 12.0\Library\Parts.I	
	Part Acceptance:	Obsolete - Replace with 39K-r0805-2%	
		Design Version: 2 Part Pin	
		Library Version: 2 Visible	
	ОК	Cancel <u>Attributes</u> Mor <u>e</u> <u>H</u> elp	

#### Let's Connect the Components together!

You can connect two components simply by placing the connecting terminals (pins) onto each other or use the Add-Connection ៉ function. Then you can drag them apart to see the connection. Pins that are connected will be automatically hidden.

CADSTAR allows you to make pin names or numbers visible/invisible so you can see which pin is number 1 or 2 (useful for engineers to see).

- Select Tools→Options→Display from the menu and enable/disable Override Part Pin n. Names/Numbers Visibility.
  - 0. CADSTAR provides an Interactive check for flagging over lapping connections. Select Tools→Options→[Interaction] tab.

When the Prevent Overlapping Connections selection is enabled, the check will alert you with the following error when you attempt to drag a connected terminal of any sort and place it on top of a connection line of a different net name.

Error	×
8	Cannot complete operation - connections on different nets overlap
	ОК

Interaction	
Paste Replaces Selection	
Copy And Paste Variant Symbols	
Copy to Bitmap	
Copy to Metafile	
Copy to Design File	
Dynamically Optimise Connections	
Auto Merge Connections	П
Prevent Overlapping Connections	
1	-
	-

If you do not wish to run the interactive check until a more convenient time, simply disable the selection. When you are ready to perform a batch check of the design, move the cursor over the Overlapping Connection active report button to make the report panel open.



Our description Connections	
Overlapping Connections	
🛛 🕅 🖆 🗇 🤋 📭 📴	
Design: C:\V: Public\Zuken\CADSTAR Express 13.0\Self	Teach\Example1.scm
Design Title:	
A4-euro -Size Sheet	
Date: Thursday, July 21, 2011	
Time: 4:46 PM	
♦ Connection on net: \$12 on sheet Sheet1	overlaps with connection on net: \$4
♦ Connection on net: \$12 on sheet Sheet1	overlans with connection on net: \$4
♦ Connection on net: \$12	overlaps with connection on net: \$4
♦ Connection on net: \$12 On sheet Sheet1	overlaps with connection on net: \$4
	overlaps with connection on net. 34
End of report	
<u> </u>	
📔 Bus Report 🗮 Design Rule Errors 🔛 Electrical Rules Check 🗜 Overlag	ping Connections 🔋 Routing Completion 😰 Unused Components
Datady	22702 5 5421 5 Thou Grid: 5 0

Click the Overlapping Connection report button as shown above and click the OK button on the report options dialog.  $\rightarrow$ 

The resulting report contents are hypertext. By selecting a line item will make the error appear in the schematic window.

Overlapping Connections	×
Report Target ✓ <u>View Report</u> <u>Print Report</u>	
🔲 <u>S</u> ave Report To File	<u>C</u> hange File Name
OK Cancel	<u>H</u> elp <u>Options</u>

p. After you have added all the components, you can add three AGND symbols. To do so, simply click the Add→Global Signal Icon ⊒ and choose (AGND). You can connect the AGND terminal and the terminal of the diode (cathode) by placing the terminals onto each other as shown below.



q. After three AGND symbols have been added, search on soldereye-1mm and add two pins. The purpose of these two pins is for the wiring connection to the battery pads; hence a pad is connected as 9V and the other AGND.

SOLDER\* 🛛 🙀 😰





- r. Change the Symbol Details name to VCC9V and AGND respectively. To change the name, select the pins 🔪 and click the Item Properties 🚺 icon.
  - s. Connect the symbols together in the same way as the hand-drawn schematic is connected electrically. To connect, click the Add→Connection 🔛 Icon.

While connecting, you can also use the right-hand mouse button to Change Default Net Route Code, allowing you to select a different Net Route Code (I like Power & GND thicker than signal tracks).

t. Change the net name connected to VCC9V to VCC by selecting the net
and clicking the Item Properties
icon.



If Automatic Version Increment in  $Tools \rightarrow Options \rightarrow [System]$  tab is enabled, with every future change of a symbol, component and part, the version increments automatically as it is saved to the library. You can easily check if a component in your Schematic or PCB design matches the current Library version. To check, click on Actions  $\rightarrow$  Reload Parts/Symbols (Components).

📲 Reload Parts/Symt	ools From Library							X
Action	Part	Instance Name	Reference Name	Alternate Name	Design Vers	ion Number	Library Version Number	Attributes
	Unallocated							D Baset Basiliana
	HLMP-1585				2		2	
	± 470E-MRS25-1%				1		1	Remove Other
	∃9K-MRS25-1%				2		2	Annouces
	10uF-10V-EC				1		1	— Betain Local
	E 2N3904				1		1	Reference Name
		TR1	S_NPN	S_NPN_1	1		1	
		TR2	S_NPN	S_NPN_1	1		1	I Reload Pin Names
	<b>⊞</b> 1N914				1		1	Reload Pin Labels
					R	eset to 0	Drigin Name	Name Yisibility       Name Yisibility       Alkways Retain       Alternate       Reset to Origin       Symbol Name       Jabel/Name       Part Name       Expand All       Contract All       Select Out of Date
					<b>V</b>	Symbol	Name	Select All
Report	Options					( diriva		Cancel Help





You can also use this function to reset all selected parts, Label, Symbol and Part name attributes to their original locations as defined in the library by selecting a *Reset to Origin* option.

- u. When completed, save this schematic design
- v. In today's market it is important to deliver a B.O.M. (Bill of Materials or in CADSTAR called Parts List) at an early stage.

To create a Parts List, simply click on **Tools**  $\rightarrow$  **Reports**  $\rightarrow$  **Parts List**. Or if you prefer to create a Parts List in a different format (fully customizable) simply click on **Tools**  $\rightarrow$  **Report Generator**  $\rightarrow$ **Manage Reports** and open the file **part\_list.rgf**, which you can find in the *Reports* directory and just click [**Run**]. You can customize the Parts List output and list any attribute (wattage, voltage, tolerance, manufacturer etc.) in any particular order you choose. For the more advanced users among you who have experience in Visual Basic or C++, you can create, for example, a user-defined B.O.M in Microsoft Office Excel, by using the OLE automation in CADSTAR.

- w. To print your schematic design, simply click on File→Print Icon and go through the Print and Page Setup. Alternatively you can print your schematic design to a PDF file, you do not need to install a PDF writer, CADSTAR has its own native PDF writer.
- **Tip:** Enable Alternative text output in the print options, making text **searchable** when printing to a file format such as **PDF**.
- x. Finally, transfer the schematic to PCB through File→Transfer to PCB. Choose '2 layer 1.6mm.pcb' as PCB Technology. Click [OK]





5	La	yers			embe layers contraction of the layers contra
Name	Thickness (Thou)	Sub Type	Physical Layer	Swap Layer	ckness = 63.0th Add Layer
Top Profiling Plat	0.0	(None)	1	(No Sw	Top Elec (0.7) Delete Layer
Top Profiling Non	0.0	(None)	1	(No Sw	Move Un
Top Placement	0.0	Placement	1	Bottom	
Top Assembly	0.0	Assembly	1	Bottom	Move Down
Top Glue Spot	0.0	(None)	1	Bottom	Calum Order
Top Paste	0.0	Paste	1	Bottom	
Top silk	0.0	Silkscreen	1	Bottom	Show Layers of Ty
Top Solder Resis	0.0	Solder Resis	1	Bottom	P Electrical
No tracks	0.0	(None)	1	(No Sw	0
No vias	0.0	(None)	1	(No Sw	
Top Elec	0.7	(None)	1	Bottom	g 🖉 🔽 Lourington (C4, C) 🔽 🔽 Non Electrical
Laminate1	61.6	(None)		(No Sw	h Laminater (61.6)
Bottom Elec	0.7	(None)	2	Top Ele	
Bottom Solder Re	0.0	Solder Resis	2	Top Sol	H Documentation
Bottom silk	0.0	Silkscreen	2	Top silk	
Bottom Paste	0.0	Paste	2	Top Pas	Physical Layers
Bottom Glue Spot	0.0	(None)	2	Top Glu	Minimum 1
Bottom Assembl	0.0	Assembly	2	Top As	Maximum
Bottom Placemen	0.0	Placement	2	Top Pla	
Mechanical Dra		(None)		(No Sw	Apply Maxim
Letter Drill Drawi		(None)		(No Sw	
Documentation		(None)		(No Sw	Bottom Elec (0.7)
thm_power_b		(None)		(No Sw	Show Picture
				Þ	Copy     All Layer Pairs     Short/Error Colour     Copper Colour     Drill Colour     Construction Colou

**Note:** If you choose the PCB Technology **'1 layer 1.6mm.pcb'** during transfer to PCB, this default technology file is prepared for single sided boards (whereas I prefer larger solder-pads, thicker track-widths and more spacing). The advantage of the different technology files is that you still can make use of ONE library as you will experience in Design D.

For an error free transfer from your schematic to PCB, no netlist is necessary!

y. If you didn't complete the schematic design as described above, just open Example1.scm and transfer the schematic to PCB through File→Transfer to PCB, choose '2 layer 1.6mm.pcb' as PCB technology.

The first step showed you how a schematic design can be drawn for Design A. In fact, any schematic capture can be drawn following the sequence shown. However, a more complicated design will require more challenging steps. There are many tools within CADSTAR Design Editor that will help designers like you to design a schematic. You can also add spacing classes, insert a component into a net without any disconnection, and perform auto-connection of busses. Other tools like Align Symbol, Design Re-use, Design Variant, Hierarchical Design, etc are also important and are user friendly for professional design engineers to use. Go ahead and try them out!

You can now move on to PCB Design. You will notice that the CADSTAR Library, Schematic and PCB design editor run on the same Graphical User Interface, guaranteeing a fast and problem free transfer.



#### Step 2 - PCB Placement for Design A

- a. You are now in the PCB Layout area with all the 12 components and 2 pins stacked on top of each other. Save the New PCB design with a file name of your choice into the ../Self teach/ folder.
- b. You should make sure that the units are set to "Thou" (Thousandth of an Inch) by selecting **Settings Units** or alternatively by double-clicking the units Thou Grid: 5.0 at the bottom of the CADSTAR window.
- c. First, you will have to draw a PCB outline;

A board outline can either be drawn within CADSTAR or imported via DXF format.

Select (*File→Import→Format →[DXF]*).

Select the DXF file *Boardoutline.dxf*.

For the Mapping-file, you have to select *dxfio.map*, which you can find in the *User* folder and just click OK.

If you have chosen to import the DXF board outline, then skip to step g.

Import Design	DXFIO.map does not include board outline	×
C:\Program F	ile\Boardoutline.dxf	<u>B</u> rowse
Format: DXF	•	Abou <u>t</u>
CAD CAD CAD	IF STAR 7 (for DOS) PCB Binary STAR 7 (for DOS) PCB Initial Data	<u>F</u> ormat Help
Mapping OrCA PCB C:\Prog PRE PRE RINF	D 'PCB' Netlist Archive ditor XR Files ditor XR HS Files Netlist	B <u>r</u> owse
C Create <u>N</u> e	w Design 📀 Merge into	Current <u>D</u> esign
[	OK Cancel <u>H</u> elp	

**Note:** the board outline that is imported using the DXF data is different from what is described in step 'd'. The intent is to demonstrate the support for DXF Line entity styles such as BLOCK, INSERT, ELLIPSE, SPLINE and POLYLINES.

CADSTAR also supports Importing and Exporting of IDF 2.0 and 3.0 from most mechanical CAD systems.

d. Alternatively you can manually draw the board outline.

Locate the Shape *quick-pick* toolbar and change the default to **Board** as shown to the right,

Next, click the "Add Rectangle" button **O C C** and begin drawing a rectangular outline (size 2000x1000 thou).

**Note:** Watch the absolute and incremental coordinates at the bottom of the CADSTAR window when drawing the board outline.

Libraries	<u>Toois window Heib</u>						
· ⊂   i	, 🏢 😋 (DEFAULT)						
Ĵ≮I	Copper 🔹	8					
le1.scm -	le1.scm - Area						
	Board						
	Copper Figure						
	Template						

**Tip:** From any point in the design you can reset the incremental coordinates by pressing the 'Z' key, followed by the [Enter] key.



e. To modify any outline (board, figures, component outlines etc), simply click on the shape edge and select one of the grab handles. You can also use the **Shape Properties** window. By selecting the outline you can see and modify the absolute or relative coordinates.



f. You can also create screw holes or mounting holes if you like. To do this within the board; locate the Shape quick-pick toolbar and change the default to **Cutout**, and click any of the drawing tool icons **C**. Click on the board outline and begin drawing a Cutout within the shape. Place a Circle Cutout in each corner of the board outline as shown above.

If you didn't manage to draw the board outline or to import the board outline through DXF, just open **Example1a.pcb** 

g. Once the board outline has been imported or drawn manually you can set an *interactive origin*, to reference all X and Y co-ordinates of all design items, and cursor positions, relative to the new origin. Select **Settings→Interactive Origin** ( and place the origin at the lower left corner of the board. When you enable **Snap to Endpoint** it will be even easier to place the Interactive Origin. To do so select **Settings→Snap→ Endpoint** 

*Note:* If the Snap toolbar is not visible, go to *Tools* ->*Customise* ->*Toolbars* and enable Snap.





#### Let's Place some Components!

Let's start by placing the critical components inside the board outline. In this sample design, the pins (for 9V and GND) and the LEDs should be placed first. You may consider these components as Critical where as their location would be described by Mechanical Engineers. This is also possible in CADSTAR using the BoardModeler Lite application. If you do not have BoardModeler Lite you can use the **Item Properties** functions to enter placement criteria such as X, Y Coordinates, Rotation and Board side. Let's Try it!

h. For this step, click the *Item Properties* **i** Icon, then select pin VCC9V by clicking on the outline or just type in "VCC9V" followed by the [Enter] command (it will be highlighted automatically), then change the X-position to 250,0 and Y-position to 875,0.

Repeat this action for:

Pin AGND, change the X-position to 450.0 and Y-position to 875.0 Component LED1, change the X-position to 250.0 and Y-position to 175.0 and rotate 90° Component LED2, change the X-position to 1750.0 and Y-position to 175.0 and rotate 90°

Tip: Choose the "*Fix*" setting to lock the components in place to avoid having them accidentally moved.

i. For the next step, select the **Embedded Place and Route Editor** <sup>™</sup> tool bar icon or select Tools→Embedded Place and Route in the menu bar.

Enter **<Ctrl+A>** to select all components.

Select the Placement  $\rightarrow$  Stack off-Board function or click the tool bar icon  $\square$ . This will result in all the components that are currently unfixed to be randomly placed around the perimeter of the outline.

j. Select the Move tool bar icon 啦 and the Component mode focus icon.



Select the component "TR1" and move the cursor inside the board outline. Click the Right Mouse Button and you will see a list of assist commands as shown to the right. ->



Selecting **Clockwise** or **Anti-Clockwise** will rotate the component accordingly. You can do so by pressing 'C' or 'A' on the keyboard to gain the same result.

Selecting **Swap** will mirror the component shape to the opposite placement side.

The Embedded Placement tool will aid in error free placement. However, there are times when an error is needed temporarily. Such as, to place a component back outside of the board outline temporarily. This can be achieved by toggling "**Errors Allowed**" in the "Routing Options".

If the default action is to push other components, the opposite behavior can be chosen by toggling the **Dynamic pushing** function.

To set the default action, see Settings→Placement→Push-Aside



Practice using this to achieve some preliminary results.

I. After the placement of all the *critical* components and some preliminary placement is complete, you can Exit the Embedded Place and Route Editor and place the remaining components by selecting *Actions*-*Placement*-*Automatic Placement* in the menu bar. You can *Enable* all *Auto Rotation angle* in the Automatic Placement window before placing the components (depending on your design rules). Try the different settings and experiment with the different results.



- n. If you didn't manage to place the components, just open *Example1b.pcb*
- You can also move the components manually if you wish, and change to a smaller working Grid Thou Grid: 5.0 to suit your placement needs (just double-click on the grid button at the bottom of the window).
- Note: you can select any footprint in PCB by simply selecting the particular symbol in the schematic. In CADSTAR, we call it Cross-Probing. To try it out, select *Window→New Vertical Tab Group* in the menu bar first. To continue with the next exercise, you should activate and enlarge the PCB Design window.



#### **Create a Partial Powerplane**

q. Finally to create a partial power-plane, create a template by selecting the board outline, choosing *Actions→Duplicate Shape* reactions in the menu bar and change the type to *Template* and the *Layer* to *Bottom Elec*.

*Note:* Copper pour will be generated automatically in the Embedded Place and Route or standalone Place & Route Editor on solder side based on the template area. Copper shapes will be created to fill in the empty space within the template outline connected, for example, to AGND.

r. After the template has been created, you should set the properties for this template. To do this, select the template and click on the *Item Property* icon.

You can set the properties as follows:Name Template:Bottom AGNDRelief Copper Code:10Layer:Bottom ElecSignal Name:AGNDClearance Width:10Thermal Relief:Enable On Pads (Angle45°)Note:Automatic Pour is ENABLED![These are the important parameters you need to set]

Item Properties Te	mplate - Co	oper Pour 🔀
Name: Bottom A	GND	Eixed
Line <u>W</u> idth Code:	Line 1	
Fill <u>T</u> ype:	(Clear)	
Copper Code:	10	<b>•</b>
<u>R</u> elief Copper Code:	10	· ·
Layer:	Bottom Elec	<b>_</b>
Signal <u>N</u> ame:	AGND	<b>•</b>
Clearance Width:	10.0	Allow In No Routing Areas
Additional Isolation:	0.0	Box Isolated Pins     Automatic Pour
Sli <u>v</u> er Width:	0.0	Target For Autorouting
Retain Poured Cop	per	Thermal Relief Angle
Grea	ater Than	✓ On Pads: 45.0
Solated: 0.0	)	🗖 On Via <u>s</u> : 45.0
Disjoint: 10	0.0	Relief Type: Cross
ОК	Cancel	<u>Attributes</u> <u>H</u> elp

The steps that were mentioned in this chapter are again a typical sequence. There are other tools such as Radial Placement, Gate and Pin Swap, Replicate Placement etc., to help designers like you to achieve a correct placement of components.

After the completion of the placement you can now start to route the PCB. Select **Tools → Embedded Place and Route** or click the **Embedded Place and Route** icon in the menu bar, to go to the embedded place and route environment.

If you didn't manage to create the template, just open *Example1c.pcb*, before going to the routing environment.



## Step 3 - PCB Routing for Design A

<del>ال</del>تك

You are likely to be at the Embedded Place and Router by now, but before starting any routing I advise you to check the Routing Options. Setting the Routing Options is very important before any routing!

a. Select **Tools**  $\rightarrow$  **Routing Options**... in the menu bar or click the Routing Options  $\square$  icon.

Routing Setup	$\mathbf{X}$
General Trunking Options	
Process      Route      Smooth	Interaction Ask before rebuilding Router results into layout
Options       Angle         Errors Allowed       90 Degrees • 45 Degrees • Free         On Line DRC       Active 45         Passes 10       Active 45         Effort       10         Tidy Rectangle Size:       0.0	Track Style Straight Curved Optimal Width Necked Typed 20.0 Thou
Via ✓Vias Allowed □Vias Under Single Layer Pads	Equispace Change Length With Equispace Equispace While Refine Routing
Pusher       Image: Constraint of the second s	idard
	OK Cancel Help

The "Routing Options" box contains several options for the routing process: Route Width, Routing Parameters (for autoroute), Routing Angle, On-Line Design Rule Check, Push Aside, Activ-45 Degree Routing etc. Make sure that at least On-line DRC, Angled Autorouting, Angle 45 Degrees, Activ-45 Degree Routing are *Enabled*. You can use these options to create the result you want.

- b. You can start with manual routing by clicking two icons on the toolbar, Item Focus in and Manual Route is as shown. Try out the Activ-45 Degree Routing and Automatic Pour starting on the Solderside (Bottom Elec), by selecting a net just once and moving the cursor to the other end of the net quite easy!
- c. You can change the active routing layer from Top Elec Top Elec to Bottom Elec Bottom Elec (by clicking the Top Elec button at the bottom of the window and changing the current layer to Bottom Elec).
- d. While routing, you can insert a Via by using the right-hand mouse button and select Change Layer.



- e. You can change the route width on the fly from Optimal to Necked or Change Width using the right-hand mouse button and select Change Width (you can choose a width between Min and Max, depending on your Route Assignments).
- f. You can also use the automatic routing features (usually designers like you will leave this step to the last, as manual or semi-automatic routing is usually necessary for the critical nets/connections). The two icons used are Net Focus I and Autoroute and you can autoroute either by net or just drag an area around the whole board outline.
  - g. Copper pour will be generated automatically on solder side (Bottom Elec), saving lots of time! When you have enabled automatic pour!!!

**Note:** the copper poured into the template will have followed the properties you have set. The copper will also have automatically avoided the cut-out of the board outline.

After completion, you can go back to the PCB Design Editor window by selecting File→Exit Embedded Place and Route in the menu bar or by clicking the Exit Embedded Place and Route
 icon. Don't forget to rebuild the router results into the layout. You can now see a design similar to the PCB shown below.



i. For a different view of the PCB use the View→Mix Colours (transparency) mode. This will display multiple layers so that all items are visible.

**Note:** This is best viewed using a Black Background.

- j. If you required a mirrored view of the PCB design you may select View→Mirrored View. This view option allows work to be performed as if you are working on the bottom side of the PCB.
- k. At this stage, you can save the file 📕

If you didn't manage to route the design, just open Example1d.pcb to have a look.

This is probably the last stage of the PCB design. It requires some careful considerations as to how the board can be routed, what are the critical nets and what nets have to be routed manually etc. For advanced users, more routing features and high-speed routing are to be considered.





## Step 4 - Manufacturing data for Design A

At this stage, you can also create the manufacturing data (Gerber, N.C.Drill, Parts List, Placement data, Drill Drawing, etc.) for the manufacturing of the PCB. If you want to output the coordinates in millimeters you have to change the Units by selecting Settings  $\rightarrow$  Units in the menu bar.

Let's start by creating a Drill drawing with an associated Drill table as shown below..



Drill holes marked with letters that correspond to a hole count in a table or legend.

a. Load the colour file called Drill Drawing. This is found in the pull-down menu adjacent to the colour palette Icon.

> This can also be loaded by typing [col drill drawing <enter>] at the command line

b. Select the Settings→Drill Letters/Table function.

Prill Letters and Drill Table						
Drill Drawing Drill Table Drill Letters						
Manual Drill Letter Association Automatic Drill Letter Association:						
Q 0.0 · 0.0 ▲ Automatic Drill Letter Association						
A         13.0         5         0.0           B         20.0         -         0.0           C         24.0         -         0.0						
E 32.0 - 0.0 F 39.0 - 0.0 F 39.0 - 0.0						
G 47.0 - 0.0 H 63.0 - 0.0 I 71.0 - 0.0 I 71.0 - 0.0						
J 79.0 - 0.0  Cutput Slotted Holes						
L 94.0 - 0.0 Conly Dutput Slotted Holes						
N 110.0 - 0.0 0 118.0 - 0.0 P 126.0 - 0.0						
Q 130.0 - 0.0 I Layer Pairs						
Code: (Through Hole)						
Change Drill Diameter						
Selections File						
Open Save as Defaults						
OK Cancel <u>H</u> elp						



Select Automatic Drill Letter Association option as shown.



c. Select the **Settings→[Drill Table]** tab.

d.

- Drill Letters and Drill Table × Drill Drawing Drill Table Drill Letters Position Properties Origin Fixed Position Х  $\mathbf{C}$ C  $\odot$ Mirrored  $\circ$  $\odot$ 0 Y œ C C Orientation 0.0 Ŧ Layout Control Lay Letter Drill Drawing -Text Size 50/50/10 • Text Code Add Drill Table • Line 5 Line Code (Border) • Line Code (Grid) Line 5 Show Drill Settings ОΚ Cancel <u>H</u>elp
- e. Select the Show Drill Settings option. This will show pertinent settings that are useful for the Fabrication of the PCB.

Change the Layout, Layer

to Letter Drill Drawing

- f. Click to [Add Drill Table] button. This will make the drill table appear on your cursor.
- g. Move the table to the right of the PCB board outline and <click> to release it as shown below.



Drill Table						
Size	Length	Pla te	Through	Letter	Count	
19.7	0.0		YES	Α.	L .	
27.6	0.0		YES	8	B	
31.5	0.0		YES	C	16	
35.4	0.0		YES	ם	4	
39.4	0.0		YES	E	2	
Units-Thou, Drill Optimisation-N, Slotted Holes-N, Only Slotted Holes-N, Layer Pairs-(Through Hole), include Equivalents=N						





- h. You can continue and select File → Manufacturing Export → Batch Process # in the menu bar.
  - i. In the Batch Process window you select [Open] and choose *Manufacturing Output 2 Layer.ppf*, which you can find in the ../Self Teach/ directory, then click [START].

You can easily add more rows to create layers that you would like to post-process. In this design, since it is a 2-layer board, the layers that are to be generated are;

- Top Elec
- Bottom Elec,
- Top Solder Mask,
- Bottom Solder Mask
- Top Silkscreen

(all in Extended Gerber RS274-X format).

👹 Batch Process - [C:\Users\Public\Zuken\CAD5TAR Express 13.0\Self Teach\Manufacturing Output 2 Layer.ppf *]										
Γ	Us	e Description	Variant	Process Type	Colour/Report File	Device Type	Device	Selections	Output	New
1	<b>N</b>	Gerber Copper pattern Component	<no td="" va<=""><td>Artwork</td><td>Top Elec.col</td><td>Photo PI</td><td>rs274-x.usr</td><td>Artwork.sel</td><td>Gerber-Cu-Co</td><td><u>O</u>pen</td></no>	Artwork	Top Elec.col	Photo PI	rs274-x.usr	Artwork.sel	Gerber-Cu-Co	<u>O</u> pen
2	<b>N</b>	Gerber Copper pattern Solderside	<no td="" va<=""><td>Artwork</td><td>Bottom Elec.co</td><td>Photo PI</td><td>rs274-x.usr</td><td>Artwork.sel</td><td>Gerber-Cu-Sol</td><td></td></no>	Artwork	Bottom Elec.co	Photo PI	rs274-x.usr	Artwork.sel	Gerber-Cu-Sol	
3	<b>N</b>	Gerber Solderresist Componentsid	<no td="" va<=""><td>Artwork</td><td>Top solder ma</td><td>Photo PI</td><td>rs274-x.usr</td><td>Artwork.sel</td><td>Gerber-Solderr</td><td>Save</td></no>	Artwork	Top solder ma	Photo PI	rs274-x.usr	Artwork.sel	Gerber-Solderr	Save
4	<b>v</b>	Gerber Solderresist Solderside	<no td="" va<=""><td>Artwork</td><td>Bottom solder</td><td>Photo PI</td><td>rs274-x.usr</td><td>Artwork.sel</td><td>Gerber-Solderr</td><td></td></no>	Artwork	Bottom solder	Photo PI	rs274-x.usr	Artwork.sel	Gerber-Solderr	
5	<b>v</b>	Gerber Silkscreen Componentside	<no td="" va<=""><td>Artwork</td><td>Top silk scree</td><td>Photo PI</td><td>rs274-x.usr</td><td>Artwork.sel</td><td>Gerber-Silkscr</td><td>Sa<u>v</u>e As</td></no>	Artwork	Top silk scree	Photo PI	rs274-x.usr	Artwork.sel	Gerber-Silkscr	Sa <u>v</u> e As
6	<b>v</b>	PDF Assembly Componentside	<no td="" va<=""><td>Artwork</td><td>Top Assembly.</td><td>PDF File</td><td><none></none></td><td>pdf.sel</td><td>PDF-Assembly</td><td></td></no>	Artwork	Top Assembly.	PDF File	<none></none>	pdf.sel	PDF-Assembly	
7	<b>v</b>	Partlisting	<no td="" va<=""><td>Report</td><td><parts list=""></parts></td><td>Text File</td><td><none></none></td><td><none></none></td><td>Partslist.rep</td><td></td></no>	Report	<parts list=""></parts>	Text File	<none></none>	<none></none>	Partslist.rep	
8	<b>v</b>	Placementdata	<no td="" va<=""><td>Report</td><td>Placement2.rg</td><td>Text File</td><td><none></none></td><td><none></none></td><td>Placement.rep</td><td>Add Ro<u>w</u></td></no>	Report	Placement2.rg	Text File	<none></none>	<none></none>	Placement.rep	Add Ro <u>w</u>
9	<b>v</b>	Drilldata (Plated Through Holes)	<no td="" va<=""><td>N.C. Dri</td><td>Defaults.col</td><td>NCDrill</td><td>excellon2.u</td><td>Drill_Plated.se</td><td>Drill-Plated.drl</td><td></td></no>	N.C. Dri	Defaults.col	NCDrill	excellon2.u	Drill_Plated.se	Drill-Plated.drl	
10	<b>v</b>	Drilldata (Non-Plated Through Hole	<no td="" va<=""><td>N.C. Dri</td><td>Defaults.col</td><td>NCDrill</td><td>excellon2.u</td><td>Drill_NonPlate</td><td>Drill-Non-Plate</td><td>Delete <u>R</u>ows</td></no>	N.C. Dri	Defaults.col	NCDrill	excellon2.u	Drill_NonPlate	Drill-Non-Plate	Delete <u>R</u> ows
11	<b>N</b>	PDF Drill Drawaing	<no td="" va<=""><td>Artwork</td><td>Drill Drawing.c</td><td>PDF File</td><td><none></none></td><td>pdf.sel</td><td>Drill_drawing.</td><td></td></no>	Artwork	Drill Drawing.c	PDF File	<none></none>	pdf.sel	Drill_drawing.	
										☑ Hjde Dialog E <u>di</u> t File
Output Directory:       C:\Users\Public\Zuken\CADSTAR Express 13.0\Output\       Extensions										
	R <u>e</u> port.						Chec <u>k</u> P(	CB <u>S</u> tart		Help
Ready	eady.									

Other additional manufacturing data that CADSTAR can generate which is necessary for manufacturing are;

- Parts Lists,
- Placement Data
- Drill Drawing
- Extended Drill Data

All manufacturing data will be saved in the Output directory.

There are other tools such as Associated Dimensioning (Orthogonal, Angular, Radial etc.), Snap, Component Rename etc., to help designers like you to create all the necessary manufacturing data.





#### Step 5 – Saving your Design for future Reuse

Of course you will want to save your design, maybe even "reuse" it with other designs. CADSTAR offers functionality for managing your *reusable circuits*. This makes it possible to load the designs into a new design as a *Reusable Block*.

For instance; if you display both your Schematic and PCB Design in CADSTAR I will show you how.

- a. Select the electrical contents of your schematic using a simple framing method.
  - b. Select Actions→Reuse Blocks→Create Reuse Block. The default location for reusable blocks is in the Reuse Files folder.
  - c. Choose a valid meaningful name for the file. I.e. Flasher\_V1.SCM and then select [OK].
  - d. Enter the same name for the **Reuse Block** name.
  - e. Repeat the process for the PCB circuit data i.e. Flasher\_V1.PCB



f. Select Actions -> Reuse Blocks -> Manage Reuse Blocks. Your new block name will be listed.

Reuse Block Manager	□ Item	Copper will Block.	not be included	l in Reuse
{ All Reuse Blocks } Flasher_V1	Eile path       en\CADSTAR Express 13.0         Settings       Image: Capacity of the set	VReuse Files VFlash	Do fixed items saving the reus	become unfixed when e block?
Rename	OK Can	cel <u>H</u> elp		

**Note:** Since the Reuse Block files are named, this functionality will allow you to manage them within the \Reuse Files\ folder. If you decided to make changes to the blocks, update both the Flasher\_V1 SCM and PCB files. Then for any designs that used the Flasher\_V1 circuit, you can simply update them by double clicking on them and selecting the **Actions**→**Reuse Blocks**→**Update Reuse Block** function.

In the next project Design-B, you may insert the **Flasher\_V1.PCB** block into the PCB design during the Placement process. Simply select **Actions→Reuse Blocks→Insert Reuse Block** and select **Flasher\_V1** 

You should also add the Flasher\_V1 schematic block to the second page of your Design-B Schematic project so the Schematic and PCB will match each other.



## Congratulations on completing your first design with CADSTAR Express!

#### I hope you found this quite interesting?

#### Add the power of 3D to your design.

You can also checkout BoardModeler Lite, supporting import/export of STEPS AP203, AP214, ACIS,STL and IDF formats, providing you an optimized solution for the placement and verification of a PCB Design in its own 3D environment, including:

- a. Replacing board shapes and modifying component placements which are smoothly back annotated.
- b. Creating detailed 3D models using the 3D parts creation wizard
- c. Importing Mechanical Enclosures (or other PCB designs).
- d. Measuring Distances and Checking Clearances.
  - e. Running Batch collision checks.

#### BoardModeler Lite is more than just a 3D viewer!!!

#### You can find more information at:

http://www.zuken.com/products/cadstar/physical/board-modeler-lite.aspx



ZUKEN

For more information visit www.zuken.com/cadstar

#### • Chapter 2 – Design B



If you want to continue practicing, go on to Design B.

Transistor Audio Amp (50 mW)

#### Information on Design B - Transistor Audio Amplifier

Here is a little audio amplifier, similar to what you might find in a small transistor radio. The input stage is biased so that the supply voltage is divided equally across the two complimenting output transistors, which are slightly biased in conduction by the diodes between the bases.

A 3.3 Ohm resistor is used in series with the emitters of the output transistors to stabilize the bias current so it doesn't change much with temperature or with different transistors and diodes. As the bias current increases, the voltage between the emitter and base decreases, thus reducing the conduction.

Input impedance is about 500 Ohm and voltage gain is about 5 with an 8 Ohm speaker attached. The voltage swing on the speaker is about 2V without distorting and power output is in the 50mW range. A higher supply voltage and the addition of heat sinks to the output transistors would provide more power. The circuit draws about 30mA from a 9V supply.



# Step 1 - Schematic for Design B

In Design B, you will have to decide what to do based on the knowledge you have gained from your work on Design A. I will guide you through it to give you some tips. The sequence is the same as Design A.

- a. Study the schematic.
- b. Collect and note information on the components.
- c. From the hand-drawn schematic, you should be able to locate the eighteen (18) components needed. They are:

Qty. per Part

- 2 2N3053 NPN Transistor
- 1 2N2905A PNP Transistor
- 2 1N4148 Diode
- 2 3.3 Ohm Resistor (3E3-MRS25-1%)
- 1 22 Ohm Resistor (22E-MRS25-1%) -
- 5 SOLDEREYE 1MM (for Input, Speaker and 9V supply)
- d. Create a new schematic sheet (I like Form A4-euro)
- e. Pick out components from the Library Workspace window
- f. Place the components on the schematic sheet
- g. Connect the components 🟙
- h. Change any net information (remember, I like a different *Net Route Code* for Power & GND)
- i. Save the design 퇴
- j. Create the Parts List
- k. Print the design 🔿
- I. Transfer the schematic design to PCB (choose '2 layer 1.6mm.pcb' as PCB technology)

If you didn't complete the schematic design as described above, just open *Example2.scm* and transfer the schematic to PCB through *File→Transfer to PCB*, choose '2 *layer 1.6mm.pcb*' as PCB technology.

- 1 470 Ohm Resistor (470E-MRS25-1%)
- 1 1.5k Ohm Resistor (1K5-MRS25-1%)
- 1 5.6k Ohm Resistor (5k6-MRS25-1%)
- 1 47uF/10V Elec. Cap (47uF-10V-EC)
- 1 1000uF/50V Elec. Cap (1000uF-50V-EC)







# Step 2 - PCB Placement for Design B

I assume that completing the schematic design was a breeze. You can now start to place and arrange the components on the PCB after the transfer. Again, I will give you some important points to follow in order to complete the PCB placement.

- a. Check and/or change the Units & Grid (25 thou is preferred)
- b. Change in the shape toolbar the Default Shape Type to Board
- c. Draw a board outline (size 2000x1500 thou). If you didn't manage to draw the board outline, just open *Example2a.pcb*
- d. Using **Item Properties** manually place the critical components inside the board outline:

Place VCC9V at	X-position 150.0 and Y-position to 150.0
Place INPUTGND at	X-position 150.0 and Y-position to 1050.0
Place INPUT at	X-position 150.0 and Y-position to 1350.0
Place SPK at	X-position 1850.0 and Y-position to 1350.0
Place SPKGND at	X-position 1850.0 and Y-position to 1050.0

- e. Fix the position of VCC9V, INPUTGND, INPUT, SPK and SPKGND
- f. Cross-probe if it is necessary
- g. Select the "Embedded Place and Route" tool bar button.
- h. Arrange components around the Board Outline using the Placement→Stack Off-board
- i. Select the Move tool bar icon 🙀 and the Component mode focus icon.
- j. Manually place the other components. If you didn't manage to place the components, just open Example2b.pcb
- k. Exit the Embedded Place and Route.
- I. Draw one or more templates 🔽 (remember the Duplicate Shape function and do not forget to allocate the signal name AGND to the template). If you didn't manage to create the template, just open Example2c.pcb, before going to the routing environment.
- j. Transfer the PCB to the Embedded Place and Route 🔁



# Step 3 - PCB Routing for Design B

You are now at the final stages of the PCB design. Again, simply follow the steps and you will complete your design very soon.

- a. Manually route any critical nets 🛄 🔪
- b. Automatically route all other nets 1 🗟
- c. Exit Embedded Place and Route 🛅

If you didn't manage to complete the design, just open *Example2d.pcb* to have a look.



Design B after Placement & Routing

# Step 4 - Manufacturing Data for Design B

You can select **File**→ **Manufacturing Export**→ **Batch Process** [Open] select *Manufacturing* **Output 2 Layer.ppf**) in the menu bar to create the manufacturing data.

#### WELL DONE! You have now completed the PCB design





At this point you might want to check out the capabilities of **BoardModeler Lite**. It supports import/export of STEPS AP203, AP214, ACIS STL and IDF formats; providing you an optimized solution for the placement and verification of a PCB Design in its 3D environment. You can replace the board outline, modify component placements, which are smoothly back annotated, import other PCB designs and housings, then build it all together and run a complete collision check. It's not just a viewer!



You can find more information at:

http://www.zuken.com/products/cadstar/physical/board-modeler-lite.aspx



For more information visit www.zuken.com/cadstar
# Chapter 3 - Library

The CADSTAR Library Editor ensures that design integrity is maintained between the symbol, the footprint and the part information, and also supports *multiple* libraries.

The library provided with CADSTAR Express contains only a few parts essential for the PCB designs described in this '*Do-It-Yourself Book*' and some examples of the on-line CADSTAR Libraries. More libraries are available through the *Zuken Global support* site. The *ready-to-download-and-use parts* contain all the information you require including manufacturers' part numbers. They are updated and expanded regularly with over *250,000 parts* currently available. If the part required is not already available in these libraries, you can quickly and easily design your own parts using the supplied wizards and the Graphical Library Editor. Access to the on-line CADSTAR Libraries is available as part of the maintenance contract.





# Step 1 - PCB Component / BGA Wizard

You shall start with going through the BGA Creation Wizard. The component to create is a 64 pad ball BGA.

a. Click on the Toolbar (File → New [PCB Component]) and choose the BGA Wizard in the box.

Fill in a {Component} Reference Name (for example: bga64). You can also fill in an Alternate Name (for example: reflow)

Change the units from Thousandths of an Inch to Millimeters. This is handy when you have components to create that are documented in MM or Thou.

BGA Wizard

You can fill in the component Height if you want to run a Design Rule Check on the height, which can be checked against placement areas as defined in the Design Editor, or you can run a collision check in BoardModeler Lite.

As this is a new component, the version will be 1. If *Automatic Version Increment* in **Tools**  $\rightarrow$  **Options [System]** is enabled, with every future change of the component the version increments automatically and you can easily check if the component in the design is the latest version as in the library.

## Select [Next >]

b. The second step is to enter the component dimensions:

Set B to: 15 mm Set D to: 10 mm Set E to: 1 mm Set F to: 1 mm Set Nx to: 8 Set Ny to: 8

BGA Creation Wizard							
Dimensions Enter component dimensions.							
Dimensions $ \begin{array}{c}  & & B \\  & & & N_{X} \\  & & & N_{X} \\  & & & N_{X} \\  & & & & N_{X} \\  & & & & & & \\  & & & & & & \\  & & & &$	Dimension       B (mm)       D (mm)       E (mm)       F (mm)       Nx       Ny	Value 15.000 10.000 1.000 8 8 8					
< <u>B</u> ack <u>N</u> ext> Cancel Help							

## Select: [Next >]

c. The third step is to enter a Pin One Marker detail (that will ensure the correct mounting of the device). Select in this case: Mitre, the Pin One Marker Size can be 1.0 mm and the Pin One Position should be set in the corner.



![](_page_37_Picture_15.jpeg)

d. The last step is to enter the assignments to be used for pads and outlines.

**Pads:** Choose for the Pads the pre-defined pad Code *bga64r*.

**Side:** When you are creating an SMD component seen from Top View you must select the *Min* side to place the SMD pads on component side.

**Origin:** The component *Origin* should be placed for SMD components *at centre*.

For **Silkscreen**, **Placement** and **Assembly Outlines**: The *Code* specifies the thickness of the line you are drawing. For Layer you should select a corresponding layer as shown.

**Exit Directions** pertain to how the tools in the Embedded Router and P.R.Editor will exit traces from the BGA pads.

BGA Creation Wizard
Assignments Enter assignments to be used for pads and outlines.
Pads       Image: Silkscreen Outline       Image: Top Silkscreen and Assembly Outlines         Code:       Silkscreen and Assembly Outline       Image: Top Assembly Outline         Assembly Outline       Image: Top Assembly Outline       Image: Top Assembly Outline
< <u>B</u> ack Finish Cancel Help

At this stage, you can [Finish] the wizard and the bga64 will be created.

![](_page_38_Picture_8.jpeg)

You can still modify the PCB component manually if needed. When done, save the PCB Component. Click on the toolbar *Libraries* -> *PCB Components* -- *[Save Comp]*. If the component already exists in the library you can decide to overwrite it if you wish.

![](_page_38_Picture_11.jpeg)

# Step 2 - Schematic Symbol / Block Wizard

We shall start with going through the Schematic Block Creation Wizard twice. The symbol to create is a StrataFlash® Embedded Memory device. This device is built up with 2 schematic symbols therefore we will use the multiple gate functionality.

a. Click □ on the Toolbar (*File → New* [*Schematic Symbol]*) and choose the Block Wizard in the box. You'll start first by creating the power device and then creating B the logic device in one go.

![](_page_39_Picture_3.jpeg)

b. You can choose a different template-file. In addition you can also fill in the version number (1 as this is a new symbol). [**Units**] can also be changed to suite your specification

Select [Next >]

c. The second step is to enter the symbol dimensions:

Set A to: 100 (Thou) Set B to: 100 (Thou) Set C to: 200 (Thou) Set D to: 200 (Thou) Set E to: 100 (Thou) Set F to: 100 (Thou)

Schematic Block Creation Wizard Dimensions Enter symbol dimensions.		
Dimensions $\downarrow$ $\downarrow$ $\downarrow$ $\downarrow$ $\downarrow$ $\downarrow$ $\downarrow$ $\downarrow$	Dimension           A min (Thou)           B min (Thou)           C (Thou)           D (Thou)           E (Thou)           F (Thou)	Value 100.0 200.0 200.0 100.0 100.0
→ F ←	Next> Cance	Help

## Select [Next >]

d. The third step is to add Gates, Number of Pins, define the Pin locations and to fill in the Reference Name. In addition you can also fill in the Alternate Name.

Select Gates - [Add] one Gate.

Fill in the *Reference Name* for GATE A as **RC48F4400P0VT00-P** and *Alternate Name* **POWER BLOCK** 

For GATE B you can fill in the *Reference Name* RC48F4400P0VT00

Set the *Number of Pins* to **59** and select **[Update]**.

Select the *Pin Sequence* numbers 1 until 4 by using the CTRL/SHIFT key and then drag and drop the *Pin Sequence column* to *Bottom* of GATE A, as shown to the right

Pin	Reference Name/ Side	Alternate Name/	Spacers
GATE A	RC48F4400P0VT00-P	POWER_BLOCK	Add
	Left		
	<ul> <li>Bottom</li> </ul>		Delete
1		•	
2		•	Number of Pins
3		•	
4		•	59
	Right		
	⊡ Top	L	Undata
5		•	Opdate
6		•	
1		•	Pin Information
8		•	Dead Street Sile
9		•	Read From File
10	( lassificant	•	
	DC 48E 4 400 DOV/TOO	self annual	Symbol Text
GATE D	RC40F4400P0V100	<at name=""></at>	· · · · · · · · · · · · · · · · · · ·
11			Clear All Text
12		-	
13			Gates
14		•	
15		•	Add
16		•	
17		•	Delete
18		•	
19		•	Up Down
		>	

![](_page_39_Picture_17.jpeg)

Select *Pin Sequence* numbers 5 until 10 by using the CTRL/SHIFT key, then drag and drop the *Pin Sequence column* to *Top* of GATE A as shown above.

Select the *Pin Sequence* numbers 11 until 43 by using the CTRL/SHIFT key, then drag and drop the *Pin Sequence column* to *left of GATE B* as shown above.

Select *Pin Sequence* numbers 44 until 59 by using the CTRL/SHIFT key, then drag and drop the *Pin Sequence column* to *right of GATE B.* 

Select [Next >]

e. The fourth step is to enter the Pin Name/Number and Pin Label Origins.

The position of the Pin Name/Numbers and Pin Labels are related to the final pin position.

By **default** the Wizard will place Pin Name/Number and Pin Label Origins intuitively, with Pin Names outside the block, and Pin Labels inside.

Ensure the settings are  $\rightarrow$  the same as the example.

Select [Next >]

f. The next step is to enter assignments to be used for terminals and outlines.

Pinl	Name/Label O	r <b>igins</b> I label origina			
	setup pin name ar	ia label origins			
- Die	Nomo Origino				
	Add Pin	Name Origins			
	Contra Astro	20/20/4			
	Code:  Ane	/8//8/4			
	Side	Orientation	Alignment	Offset (Thou)	Direction
	Left	0.0	Bottom Left	0.0	270
	Bottom	90.0	Bottom Left	0.0	180
			D. H. D. L.	0.0	
	Right	0.0	Bottom Right	0.0	90
Pir	Right Top Label Origins ✓ Add Pin Code: Ariel	0.0 90.0	Bottom Right	0.0	
Pir	Right Top I Label Origins	0.0 90.0 Label Origins 78/78/4	Bottom Right	0.0	
- Pir	Right Top Label Origins ✓ Add Pin Code: Ariel	0.0 90.0 Label Origins 78/78/4 Orientation	Bottom Right Bottom Right	0.0 0.0 Offset (Thou)	90 0 Direction
Pir	Right Top I Label Origins I♥ Add Pin Code: Ariel Side Left	0.0 90.0 Label Origins 78/78/4 Orientation 0.0	Bottom Right Bottom Right Alignment Centre Left	0.0 0.0 0ffset (Thou) 25.0	90 0 
Pir	Right Top I Label Origins I Add Pin Code: Ariel Side Left Bottom	0.0 90.0 Label Origins 78/78/4 Orientation 0.0 90.0	Bottom Right Bottom Right Alignment Centre Left Centre Left	0.0 0.0 0ffset (Thou) 25.0 25.0	90 0 <b>Image: Second Sec</b>
Pir	Right Top ✓ Add Pin Code: Ariel Side Left Bottom Right	0.0 90.0 Label Drigins 78/78/4 Orientation 0.0 90.0	Bottom Right Bottom Right Centre Left Centre Left Centre Right	0.0 0.0 0ffset (Thou) 25.0 25.0	90 0 0 0 0 0 0 270

	Schematic Block Creation Wizard	
Terminals: Set the	Assignments Enter assignments to be used for terminals and outlines.	
Terminal Codes to	Terminals	PL5+ PL6+ PL8+ PL8+ PL9
	Code: Terminal	PL1 PL2 PL4
Code specifies the	Orientation: 0.0 Use default	
thickness of the line drawing. You should select Symbol	Outlines	2015         PL 5         PL 5         PL 30         PL 31         PL 30         PL
Outline.	Code: Line 4	8899 PL 19 PL 39 243 24 3 8919 PL 19 PL 49 244 24 4 8012 PL 12 PL 42 PL 45 244 24 4 8012 PL 12 PL 45 244 24 5 8013 PL 13 PL 46 244 24 5 8013 PL 13 PL 46 244 24 7
<b>Origin:</b> The symbol Origin should be placed at terminal	Origin at terminal one    at centre	2015         PL 15         PL 4 5-2445         49           2016         PL 16         PL 4 5-2445         49           2017         PL 16         PL 4 5-2445         49           2018         PL 16         2018         19           2019         PL 16         2019         2019           2011         PL 19         2019         2019           2012         PL 10         2019         2019           2012         PL 10         2019         2019           2012         PL 20         2019         2019
une.	Multi-gate file Browse	<u>第954</u> 月224 第755 第255 第255 第257 第 第257 第 第 5 第 5 第 5 第 5 第 5 第 5 第 5
	<pre><back cancel<="" finish="" pre=""></back></pre>	Help

![](_page_40_Picture_12.jpeg)

At this stage, you can [Finish] the wizard and the symbols will be created.

**Note:** Select **[No]** if you are asked to set the multiple gate file, this is only needed when reading an Aldec FPGA pin list file (CSV).

Warni	ng 🔀
2	There are gates defined, however the multi-gate file is not set. Do you wish to set the multi-gate file?
	Yes No Help

- g. You can still modify the Schematic Symbols manually if needed. When done, save each
   Schematic Symbol. Click on the Toolbar or select Libraries-Schematic Symbols [Save Symbol.] If the symbol already exists in the library you can decide to overwrite it if you wish.
- h. Now you can go through the Schematic Block Creation Wizard again and create another device if you wish.

![](_page_41_Picture_5.jpeg)

## Step 3 - Parts Library Editor

Now that you have created the PCB component and the schematic symbols you can generate the Part definition that will link the schematic symbols and PCB component together.

a. Click A on the Toolbar or select Libraries → Library Editor. In the Library Editor, click on the toolbar (File → Open), browse the Library directory and open "Parts.lib".

	Parts.LIB (C: \Users \Public \Zuken \CADSTAR Express 13.0 \Library \) - Parts Library - Zuken CADSTAR Library Editor Express 💶 🗖 🗙										
8	<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>S</u> ettings <u>Libraries</u> <u>T</u> ools <u>W</u> indow <u>H</u> elp										
÷											
2											
12	濱 - 〒 500   44 24   10 部										
	Parts Definitions										
	Part Name Number Description Version Definition SPICE Part Acceptance										
	39K-MRS25-1%	2322-156-13903	Metal film resistor MRS25 39K 1%	2	39K-MRS25-1%		Obsolete - Replace with 39K-r0805-2%				
	39K-r0805-2%		Chip resistor 0805 39K 2%	2	39K-r0805-1%						
	470E-MRS25-1%	2322-156-14701	Metal film resistor MRS25 470E 1%	1	470-MRS25-1%						
	470E-r0805-2%		Chip resistor 0805 470E 2%	1	470E-r0805-1%						
	10E-r0805-2%		Chip resistor 0805 10E 2%	1	10E-r0805-1%			1			
	1K5-MRS25-1%	2322-156-11502	Metal film resistor MRS25 1K5 1%	1	1K5-MRS25-1%			1			
	1K5-r0805-2%		Chip resistor 0805 1K5 2%	1	1K5-r0805-1%			1			
	22E-MRS25-1%	2322-156-12209	Metal film resistor MRS25 22E 1%	1	22E-MRS25-1%			1			
	22E-r0805-2%		Chip resistor 0805 22E 2%	2	22E-r0805-1%			1			
	5K6-MRS25-1%	2322-156-15602	Metal film resistor MRS25 5K6 1%	1	5K6-MRS25-1%			1			
	5K6-r0805-2%		Chip resistor 0805 5K6 2%	1	5K6-r0805-1%			1			
	3E3-MRS25-1%	2322-156-13308	Metal film resistor MRS25 3E3 1%	1	3E3-MRS25-1%			1			
	3E3-r0805-2%		Chip resistor 0805 3E3 2%	1	3E3-r0805-1%			1			
	HLMP-1585 9322-018-62682 LED GREEN 3MM HLMP-1585		2	HLMP-1585		Only 10,000 pieces in Stock!	1				
	1N914		High-speed diode	1	1N914			-			
<u> </u>						-					
4	🚬 Start Page 🔠 Pa	arts.LIB ×						Þ			

b. Click on the Toolbar icon I for Edit→Add New Row

![](_page_41_Picture_11.jpeg)

c. When creating Part definitions, you must fill in both the **Part Name** and **Definition** column fields (as shown below.) In addition you can fill in the Description if you want to run a more detailed Parts List of the used components in your design.

Part definitions represent the highest level of a library part. The definition can be referenced by more than one part name. However, it is more likely that every Part definition will have only one part name due to the complexity of attributes that are trying to be used, making each part name require a unique definition.

	Parts.LIB (C:\Users\Public\Zuken\CADSTAR Express 13.0\Library\) - Parts Library - Zuken CADSTAR Library Editor Express 💶 🗖 🗙								
	<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>S</u> ettings Libraries <u>T</u> ools <u>W</u> indow <u>H</u> elp								
1									
-									
	: 🎘 🚝 🞥 🛤 👯 🤍 🦻 👬 🛤 🖳 🐘 🎬 🌃 🚾 🔛 🕨 🍉 🌗 🦻								
	Par	rts Definitions							
		Part Name	Number	Description	Version	Definition	SPICE	Part Acceptance	
		SMBJ12CA		Transient Voltage Suppressor, Birdir	1	SMBJ12CA			
		CAP 2200UF 25V AXIAL		35mm Pitch, 16mm wide	1	CAP 2200UF 25V			
		10NF-20/80% SMD0805		10NF 0805 SMD CAP (X7R)	1	10NF-20/80% SMD			
		10K-1%-CRG0805		10K CRG0805 THICK FILM 1%	1	10K-1%-CRG0805			
		5K1-1%-CRG0805		5K1 CRG0805 THICK FILM 1%	1	5K1-1%-CRG0805			
		TAJ-22U/6.3V		ELECTROLYTIC CAPACITOR TAJB2	1	TAJ-22U/6.3V			
		22K-1%-CRG0805		22K CRG0805 THICK FILM 1%	1	22K-1%-CRG0805			
		LP2937		500 mA Low Dropout Regulator	1	LP2937			
		TAJ-10.0U/6.3V		ELECTROLYTIC CAPACITOR TAJB1	1	TAJ-10.0U/6.3V			
		100E-1%-CRG0805		100R CRG0805 THICK FILM 1%	1	100E-1%-CRG080			
		100NF-20/80% SMD0805		100NF 0805 SMD CAP (X7R)	1	100NF-20/80% SM			
		4K7-1%-CRG0805		4K7 CRG0805 THICK FILM 1%	1	4K7-1%-CRG0805			
		680E-1%-CRG0805		680R CRG0805 THICK FILM 1%	1	680E-1%-CRG080			
		Example		An Example Part	1	Example		This is an Exmple part - Do not use	
									•
	1	🛛 📔 Start Page 🛛 🕮 🛛 Pa	arts.LIB ×						⊳
21	0.0								
21	0 P	arts.							

d. Select the new part name "Example"

and click on the toolbar icon <sup>™™</sup> or select **Edit→ Edit Part Definition** (or use the right mouse button menu).

From the **Component** tab, click the [**Select**] button - and choose the PCB Component (bga64) that you created by using the BGA Wizard in the previous exercise.

## Set the Name Stem to: U

The Name Stem specifies the alphabetic character(s) that will be common to all component names when this part is added to the design.

This is the prefix for the Reference Designator that will be used when the part is added to a Design.

Parts.LIB (C:\Users\Public\Zuken\CADSTAR Express 13.0\Library\) - Example - Parts Libr 🚊 🚍 🗶
Eile Edit View Actions Settings Libraries Tools Window Help
🗄 🗅 😅 🔚 🎒 👗 🖺 💼 🗙 🗠 🖂 🕴 🥅 (DEFAULT) 👘 🐺 த
[凌月歸 两則 動为 月 两則  ◎惡姑幽▶▶▶ 動为
Component Symbols Pins Gate + Pin Swapping Attributes
Name Apply
Reference: bga64
Alternate: reflow
Select
Max Electrical Pin: 64 Name Stem: U
haa64 (ceflow)
*******
Start Page 🕮 Parts.LIB 🖮 Parts.LIB - Example ×
Converting design C:\Users\Public\Zuken\CADSTAR Express 13.0\Templates\defaults.cmp

![](_page_42_Picture_10.jpeg)

e. Select the **Symbols** tab and click on the toolbar icon Repeat this for one additional row to support Gates A and B

Now you can double click in the Symbol Name field or use the right mouse button menu [**Select Symbol..**] and select, for Gate A, the symbol *RC48F4400P0VT00-P* you created by using the Schematic Block Creation Wizard in the previous exercise.

**Tip:** Start typing the symbol name and the searcher will take you quickly to the symbol name

For Gate B select the Symbol *RC48F4400P0VT00.* 

![](_page_43_Picture_4.jpeg)

Change the *Files of Type* to CSV (Comma delimited).

**Tip:** A pin list can be often downloaded from the component manufacturer's website or you can extract it from the component manufacturer datasheet in spreadsheet software (for example MS Excel).

Select the file name: *pinlist.csv* and click **[OK].** This can be found in the **../Self Teach/** folder.

If the Pin list has less pins then what in the Pins tab you will get the Warning shown below.

Warning	×
1	The import file contains less than 64 pins. Not all pins will be labelled.

![](_page_43_Picture_10.jpeg)

or select Edit→Add New Row.

![](_page_43_Picture_11.jpeg)

The next step is to select pins 1 - 8 in the **Name** column and select **Actions**  $\rightarrow$  **Name Pins** g. (BGA's have Pin-Names instead of Pin-Numbers!). (You can also select this from the Right Mouse Button menu)

Enter for the First Pin Name the value: A1 and click [OK]. The pin names should appear as shown.  $\rightarrow$ 

Note: If you click in the Name cell for pin 9, you will see 'A9' fill the cell. This is the Increment continuing as defined.

C	Com	ponent	Symbo	ols Pin	s	Gate + Pin Swapping Attributes
F	Pin	Name	Label	Signal	Те	Alphanumeric Pin Names
	1	A1 👘	A1			
	2	A2	A6			Eirst Pin Name A1 O Decrement
	3	A3	A8			
	4	A4	VPP			OK Cancel Help
	5	A5	A13			
	6	A6	VCC			
	7	A7	A18			
	8	A8	A22			
	9		A2			
	10		VSS			<b>•</b>

Select pins 9-16. Click the <RMB> and select Name Pins. Enter B1 and click [OK]

Repeat this action for the Pins:

17 - 24 starting with C1 25 - 32 starting with D1 33 - 40 starting with E1 41 - 48 starting with F1 49 - 56 starting with G1 57 - 64 starting with H1

When you used the Schematic Block Wizard for the creation of the first symbol (RC48F4400P0VT00-P) a total of 10 terminals were placed on the bottom and top side of the symbol and if you remember, they are always numbered from left to right. Usually the VSS is placed at the bottom of the power symbol and the VCC at the top.

![](_page_44_Figure_8.jpeg)

![](_page_44_Picture_9.jpeg)

A1 • A2

![](_page_44_Picture_11.jpeg)

h. The next step is to map the symbol terminals with the accompanying **Pin Numbers/Names** (and Labels).

In other words you will start with the pin/ball *B2* (Label *VSS*) assigning it to Terminal A.1 = {Gate A. symbol terminal 1}

Select the Terminal field belonging to Pin Name B2 (Label VSS), and select Edit→ Assign Terminals

or use the right mouse button menu and select **Assign** 

Now you can finish the mapping for the power symbol by selecting, in the correct order, the next power pins.

![](_page_45_Figure_6.jpeg)

Look for pin/ball *H*2 (Label *VSS*) and just click in the terminal field. You will notice that automatically A.2 will be assigned.

Tip: If you make a mistake during the allocation of the terminals, don't worry - just press the [Escape] key and restart in the correct box with the new start sequence!

Now assign the following:

- pin/ball H4 (Label VSS) assign to A.3
- pin/ball H6 (Label VSS) assign to A.4
- pin/ball A4 (Label VPP) assign to A.5
- pin/ball A6 (Label VCC) assign to A.6
- pin/ball H3 (Label VCC) assign to A.7
- pin/ball D5 (Label VCCQ) assign to A.8
- pin/ball D6 (Label VCCQ) assign to A.9
- pin/ball G4 (Label VCCQ) assign to A.10

**Note:** As you Assign the terminals the Pin labels will appear on the **Gate A** symbol in the preview pane

![](_page_45_Picture_19.jpeg)

![](_page_45_Picture_20.jpeg)

Continue assigning the terminals for Gate B (RC48F4400P0VT00). Just click in the terminal field of pin/ball A1 (Label A1) and you will notice that automatically  $B.1 = \{Gate B .Symbol Terminal 1\}$  will be assigned.

When you used the Schematic Block Wizard for the creation of the second symbol (*RC48F4400P0VT00*), a total of 49 terminals were placed at the left and right side of the symbol and if you remember, they are always numbered from top to bottom.

#### You can assign following pins/balls for Gate B:

- pin/ball A1 (Label A1) assign to B.1 - pin/ball B1 (Label A2) assign to B.2 - pin/ball C1 (Label A3) assign to B.3 - pin/ball D1 (Label A4) assign to B.4 - pin/ball D2 (Label A5) assign to B.5 - pin/ball A2 (Label A6) assign to B.6 - pin/ball C2 (Label A7) assign to B.7 - pin/ball A3 (Label A8) assign to B.8 - pin/ball B3 (Label A9) assign to B.9 - pin/ball C3 (Label A10) assign to B.10 - pin/ball D3 (Label A11) assign to B.11 - pin/ball C4 (Label A12) assign to B.12 - pin/ball A5 (Label A13) assign to B.13 - pin/ball B5 (Label A14) assign to B.14 - pin/ball C5 (Label A15) assign to B.15 - pin/ball D7 (Label A16) assign to B.16 - pin/ball D8 (Label A17) assign to B.17 - pin/ball A7 (Label A18) assign to B.18 - pin/ball B7 (Label A19) assign to B.19 - pin/ball C7 (Label A20) assign to B.20 - pin/ball C8 (Label A21) assign to B.21 - pin/ball A8 (Label A22) assign to B.22 - pin/ball G1 (Label A23) assign to B.23 - pin/ball H8 (Label A24) assign to B.24 - pin/ball B6 (Label A25) assign to B.25

- pin/ball B4 (Label 'CE') assign to B.26 - pin/ball C6 (Label 'WP') assign to B.27 - pin/ball D4 (Label 'RST') assign to B.28 - pin/ball E6 (Label CLK) assign to B.29 - pin/ball F6 (Label 'ADV') assign to B.30 - pin/ball F7 (Label WAIT) assign to B.31 - pin/ball F8 (Label 'OE') assign to B.32 - pin/ball G8 (Label 'WE') assign to B.33 - pin/ball F2 (Label DQ0) assign to B.34 - pin/ball E2 (Label DQ1) assign to B.35 - pin/ball G3 (Label DQ2) assign to B.36 - pin/ball E4 (Label DQ3) assign to B.37 - pin/ball E5 (Label DQ4) assign to B.38 - pin/ball G5 (Label DQ5) assign to B.39 - pin/ball G6 (Label DQ6) assign to B.40 - pin/ball H7 (Label DQ7) assign to B.41 - pin/ball E1 (Label DQ8) assign to B.42 - pin/ball E3 (Label DQ9) assign to B.43 - pin/ball F3 (Label DQ10) assign to B.44 - pin/ball F4 (Label DQ11) assign to B.45 - pin/ball F5 (Label DQ13) assign to B.46 - pin/ball H5 (Label DQ13) assign to B.47 - pin/ball G7 (Label DQ14) assign to B.48 - pin/ball E7 (Label DQ15) assign to B.49

![](_page_46_Picture_5.jpeg)

![](_page_46_Picture_6.jpeg)

Component Symbols Pins Gate + Pin Swapping Attributes s Piliji Select the Gate + Pin Swapping Element: 10 pins RC48F4400P0VT00-P(POWER BLOCK)-A tab and click on the External External Swapping Group RC48F4400P0VT00-B Swapping Group containing 49 Element: 49 pins RC48F4400P0VT00-B Pin 1 "A1" {A1} Terminal B.1 Pin 9 "B1" {A2} Terminal B.2 pins then expand the Element contained within. Pin 17 "C1" {A3} Terminal B.3 Pin 25 "D1" {A4} Terminal B.4 Eguivalent Pins Pin 26 "D2" {A5} Terminal B.5 Select the pins with the labels {*A1*} Create Swap Element Pin 2 "A2" {A6} Terminal B.6 - {A25} as shown and click on the Pin 18 "C2" {A7} Terminal B.: Pin 3 "A3" {A8} Terminal B.8 toolbar icon Pin 11 "B3" {A9} Terminal B.9 or select Right Pin 19 "C3" {A10} Terminal B.10 Remove All Swapping Mouse Button menu  $\rightarrow$ Pin 27 "D3" {A11} Terminal B.11 Set Default Swapping Pin 20 "C4" {A12} Terminal B.12 **Equivalent Pins** Pin 5 "A5" {A13} Terminal B.13 Make Gates Identical Pin 13 "B5" {A14} Terminal B.14 Repeat the action for the pins with Pin 21 "C5" {A15} Terminal B.15 Import Multigate data Pin 31 "D7" {A16} Terminal B.16 the labels DQ0 - DQ15. If you do Pin 32 "D8" {A17} Terminal B.17 so it will help you to optimize the Pin 7 "A7" {A18} Terminal B.18 Pin 15 "B7" {A19} Terminal B.19 routing pattern in the Design Editor Pin 23 "C7" {A20} Terminal B.20 and/or P.R.Editor XR. Pin 24 "C8" {A21} Terminal B.21 Pin 8 "A8" {A22} Terminal B.22 Pin 49 "G1" {A23} Terminal B.23 Pin 64 "H8" {A24} Terminal B.24 Select the **Attributes** tab and click m. Pin 14 "B6" {A25} Terminal B.25 Pin 12 "B4" {'CE'} Terminal B.26 on the text field Value. Add the Heel Runn value RC48F4400P0VT00.

You can fill in more attributes if you like. Attribute values can be set as *Read Only* so you can't change their value in the Design Editor.

Tip: You can create user-defined attributes by clicking on the Settings -> Attribute Names.

🛛 🔀 Start Page 🕮 Parts.LIB 🖮 Pa	arts.LIB - Example X		
Component Symbols Pins Gate + Pin Swap	oing Attributes		
Attribute	Text	Read Only	Туре
Value	RC48F4400P0VT00	Yes	Symbol and Component
₩attage		No	Symbol and Component
Tolerance		No	Symbol and Component
Voltage		No	Symbol and Component
Height/Inches		No	Part Definition
Availability		No	Symbol and Component
Alternative Part		No	Symbol and Component
Price		No	Symbol and Component
Manufacturer		No	Symbol and Component
Manufacturers Part Number		No	Symbol and Component
link Manufacturer		No	Part Definition
link URL to manufacturers PDF datasheet		No	Part Definition
link On-line CADSTAR Datasheet		No	Part Definition
Designed		No	Symbol and Component
Designer		No	Symbol and Component
Sign Off Date		No	Symbol and Component
Signed Off		No	Symbol and Component
Automatic insertion		No	Component
Package	bga64	Yes	Part Definition
Technology		No	Part Definition
	1	NI-	D-4 D-6-35-

If you finished adding a part click on the Toolbar **File**→ **Save** and **Close** the file.

If you didn't manage to add the part without errors or warnings you can browse the Library folder ......\Zuken\CADSTAR Express 13.0\Library and delete the Parts.lib. Then rename the file Parts.bak to Parts.lib and repeat the last action in the Library Editor to click on the Toolbar Libraries Parts and select [Parts Index]. You should have no errors or warnings.

![](_page_47_Picture_6.jpeg)

![](_page_48_Picture_0.jpeg)

Congratulations on creating your first complex part in CADSTAR!

Why not try and add it to a sample schematic?

![](_page_48_Picture_3.jpeg)

![](_page_49_Picture_0.jpeg)

# CADSTAR FPGA

If you want to skip most steps as described above you can also use a CSV (Aldec FPGA Data) file.

To learn more you can check out **CADSTAR FPGA**, supporting Actel, Altera, Lattice, Quicklogic and Xilinx flows from one universal project manager that controls all the design files for simulation, synthesis, place and route and pin assignment to the PCB.

Pin synchronization is often far from optimal for PCB routing; this new integrated solution supports the I/O synchronization between the FPGA device and the PCB board. CADSTAR FPGA supports forward- and back-annotate pin assignment changes in order to optimize PCB routing.

*Note:* In the movies we will use a bga363 package, but for the following exercises you need to use the bga64 package. The principal is the same!

- a. You can run the Schematic Symbol Block Wizard again and read this time the pin list of the StrataFlash® Embedded Memory device as exported by Active-HDL from Aldec. Choose the file format CSV (Aldec FPGA Data) and select the file 'Aldec\_pinlist.csv'. This time export as well a Multi-gate file using the Schematic Symbol Block Wizard that will help you to create the CADSTAR FPGA Part almost automatically.
- b. Create a CADSTAR FPGA Part using the Multi-gate data file (CSV) as created by the Schematic Symbol Block Wizard. The package does already exist in the PCB Component Library bga64 (reflow).
- c. Add the FPGA device into your schematics design, transfer to PCB, place the components, optimize your PCB routing by swapping pins on the fly in the Place & Route Editor and back annotate to your schematics and the FPGA device.

A new collaborative product combining Aldec's; Active-HDL Lite and Zuken's CADSTAR in one universal project manager.

You can find more information at:

http://www.zuken.com/products/cadstar/system/fpga.aspx

If you require any support during evaluation, please contact your local CADSTAR distributor.

http://www.zuken.com/products/cadstar/where-to-buy.aspx

![](_page_49_Picture_14.jpeg)

![](_page_50_Picture_0.jpeg)

## • Chapter 4 – Design C (Standalone Place & Route Editor)

Design C has been created for the more advanced users, allowing you to make use of the Standalone Place & Route Editor XR2000. Power Users of CADSTAR tend to prefer the more powerful features such as those available within the Standalone P.R.Editor XR2000, which provides placement and routing functionality and much more. By the way, all exercises completed for Design A and Design B in the Embedded Place & Route solution, can as well be designed in the Standalone Place & Route Editor XR2000!

Also in this design we will learn how to create an Intelligent Bus and the use of Signal Reference Links.

# **Step 1 - Schematic for Design C**

To keep it simple I have already draw most of the schematics of Design C for you. Just open *Example3a.scm.* 

CADSTAR is capable of creating intelligent busses; you can restrict the signals connecting to a bus according to the signal names. The property sheet for a bus contains a signal tab where connections to a bus can be defined. If you set a bus to be none restrictive you can connect any net.

Signal reference links are used to view and 'jump' to the other signal references of the same net throughout the (hierarchical) design.

a. We shall start to create an intelligent address (AD0-7) bus on sheet 1 between U1, U2 and U3, by selecting Add→Bus

![](_page_50_Picture_9.jpeg)

Select the start point for this bus and draw the bus. To insert a corner click left mouse button, to finish the bus double click the left mouse button.

b. To add the bus name and signal names to the bus, select the bus is and click the **Item Properties** icon, fill in the bus name **AD0-7**,

neral Signals		
Bus	Transfer Bus to PCB	_
✓ Restrictive	Fixed On "transfer	
Line Code: Line 15	Transfer with all nets	
Segment(s) Length: 1450.0	Attributes O Transfer with some nets Choose Nets	
Bus Name		
AD0-7	Position: 22317.5 7467.5	
	Orientation: 0.0	
	Use Alignment       Alignment       O       <	
<	Text Code: Text Size 60/50/8	
	OK Cancel H	elp

![](_page_50_Picture_13.jpeg)

![](_page_51_Picture_0.jpeg)

Select the Signals TAB, click on Add and fill in *AD[0-7]* then press OK.

c. You can now connect connections to the bus. Select 🔪 U3-B select the **Move** 🔅 icon and move U3-B towards the bus until the terminals are on top of the bus, drop U3-B by pressing the left mouse button, the next window pops up

Auto Connect to Bus

Start Signal Name:

Start Pin Position: End Pin Position:

Connecting between Symbol 'U3-B' and Bus ".

9

2

ОK

Set this window as follows: Start Signal Name: AD0 Start Pin Position: 9 End Pin Position: 2 Press OK

Move U3-B back to its original position

Repeat this for U1-B and U2-B

To	connect	sinale	connections	to	the	hus	
10	COLLICCT	Single	001110000010113	ιU	uic	Duo	

select the Add-Connection is licon, start at the pin to be connected, than drag the wire to the bus and single select to finish. The system will ask which signal name to add.

d. Signal reference links are used to view and/or 'jump' to another associated signal reference elsewhere in the design. The visibility and format of the link is configured via the **Settings**→**Defaults** *dialog under the links tab.* 

Defaults X
General Shape Text Connection Pin Bus Link
Link Defaults
✓ Use Signal Reference Links
Properties           Code:         Ariel 39/39/4
Angle: 0.0
Formatting         Style         O Zone         O Zone         O Sheet         Sheet         Sheet         Sheet, Zone         Link Separator:         O Zone, Sheet         Maximum Line Length:
OK Cancel Help

![](_page_51_Picture_10.jpeg)

~

Help

Cancel

Horizontal Start Coordinate: 44 End Coordinate: 73 Number of Zones: 6 Start Character: 1	18.000
Start Coordinate:44End Coordinate:73Number of Zones:6Start Character:1	¥8.000 35.000
End Coordinate:73Number of Zones:6Start Character:1	\$5.000
Number of Zones:6Start Character:1	
Start Character: 1	
Size of Zone: 47.	833
Vertical	
Start Coordinate: 23	35.000
End Coordinate: 35	5.000
Number of Zones: 4	
Start Character: A	
Size of Zone: 50.4	000
Apply to All Sheets Get Coordinates	s from Sheet
Refe	erence
Text Size 75/75/12	Horizontal-Vertical
-	Vertical-Horizontal
Right Top Bottom	
	✓ Right     ✓ Top     ✓ Bottom       OK     Cancel     Help

### Set the Reference setting to Horizontal-vertical and select [OK]

Now check the signal reference VCC in the lower left corner of the sheet it should look like this

![](_page_52_Picture_3.jpeg)

You are now able to jump to the several VCC reference links in this design by double clicking on for example 1:6B or by selecting the Signal Reference  $\checkmark$  then pressing the right mouse button and selecting one of the reference links.  $\rightarrow$ 

If you don't see the Signal Reference Links, just open *Example3.scm* to have a look.

e. Transfer the schematic to PCB through **File→Transfer to PCB**, choose '*Eurocard-160x100.pcb*' as PCB technology. If you didn't manage to transfer the schematics design, just open Example3a.pcb before going to Step 2.

![](_page_52_Picture_7.jpeg)

![](_page_52_Picture_8.jpeg)

## Step 2 – Placement for Design C

a. Before transferring to Standalone Place & Route Editor XR2000, create a rough manual placement here in the Design Editor. Place all IC's as shown below. SMD components can be easily placed on both layers, select capacitor C1 (you have many options to do so), move C1 to the preferred place, click the right mouse button and select '*Mirror*' from the pull down menu. Place all capacitors at the solder side of the board.

![](_page_53_Figure_2.jpeg)

**Note:** The color of components when swapped to the other side of the board, do change! If you didn't manage to place the components, just open *Example3b.pcb* before moving on.

**Tip**: to see highlighted the nets that connect to an component. press "T" on the keyboard to toggle the associated nets to a Highlighted color.

b. Some connections between U1 and U2 are crossing! To solve this, select Actions→Gate and Pin Swap→Automatic Gate and Pin Swap and select [Start] [<sup>1</sup>].

**Note:** You can also swap pins on the fly in the Standalone Place & Route Editor XR2000. Try it!

Gate and Pin Swap	×
Type of Swap	When to Stop
Gate Swap	<u> <u> R</u>un to Completion </u>
🔽 <u>P</u> in Swap	C Summary After Each Pass
Choose <u>N</u> e	ets to Minimise
What to Swap	Swap <u>Fixed</u> Items
C Selected Compone	nts
⊙ <u>W</u> ithin Area : [Boa	ard Outline) 💌
<u>S</u> tart	Cancel <u>H</u> elp

![](_page_53_Picture_8.jpeg)

Using CADSTAR you can decide to use schematics as master or the PCB design as master. CADSTAR supports full back annotation. No matter what your choice will be, do not forget to run a **Back Annotation** when you have changed something in your PCB design, like pin and gate swap, renamed components, added, modified or deleted components, connections or attributes. If you didn't manage to do Gate and Pin Swap, just open **Example3c.pcb** before going on.

c. Open the schematics design Example3.scm
 and select File→Back Annotation

In the Back Annotation window select the PCB design *Example3.pcb* as source.

If you have added new components in the PCB design that do not exist in the Schematics you can select the sheet on which you want to add these components (in this case just select *Sheet1*).

The exclusion file can contain components that do not exist in the schematics, like mechanical holes or other components that you don't want to appear in the schematics. Just select *Example3.cig.* 

Now select [OK] to run the back annotation.

Back Annotation 🔀
Back Annotation Source C:\Users\Publi\Example3.pcb
Perform initial Back Annotation with detected RINF file
Add new symbols on sheet
Sheet1 Select
Comparison Options
Exclusions Advanced Configuration
Perform Library Reload on completion
🔽 Retajn Local Reference Name
<u>R</u> etain connection paths (add danglers) on symbol deletion
Always add Single Node Connections
Update Pin Labels
I Iranster Reuse Blocks
Perform Update of Reuse Blocks on completion
Remove Items after successful completion
Image:
<ul> <li>✓ Unconnected buses</li> <li>✓ Disconnected blocks</li> </ul>
Source PCB Options
□ Update ⊻ariant Hierarchy
Replace <u>N</u> et Route Codes
Net Route Code Assignments
Heplace Min/Max Hestrictions     Replace Optimal/Necked Widths
OK Cancel <u>H</u> elp

d. Open *Example3c.pcb* and go to the Standalone Place & Route Editor XR by selecting
 Tools→PREditor XR IS

When transferring to the P.R.Editor a *RIF Export Option* window will be showed automatically.

Be sure to enable Always Transfer Colours.

Select [OK]

RIF Export Options
Always Transfer Colours
Use Routing Grid as System Grid
Write Part Information
Write Jumpers from Library
Show this dialog on transfer to PREditor XR (HS) as well as through File Export/Options
OK Cancel <u>H</u> elp

![](_page_54_Picture_12.jpeg)

# Step 3 - PCB Routing for Design C

Welcome to the Standalone Place & Route Editor XR Environment!

![](_page_55_Picture_2.jpeg)

I▼ Springback Preview	Allow Segment Breaks
escription:	Always Generate     Auto
Open Save As	OK Cancel Help

![](_page_55_Picture_4.jpeg)

P.R.Editor cannot not only be used for routing your design, but also for changing your placement without the need to go back to the Design Editor. Before starting any placement I advise that you check the **Interactive Move** and **Push Aside** options.

b. Set the options for moving components by selecting Configure→Interactive Move in the menu bar

Setting the placement functions behavior is very important before any placement is started.

- C. Select Configure→Placement→Push Aside in the menu bar. Ensure the settings are equal to the example.
- d. Select a component and click the **Move** tool bar icon . Notice that other components are being *pushed aside* and when there is enough space the selected component jumps over other components. Components can also be swapped to the other side of the board or rotated . This can also be performed using the Right Mouse Button menu.

As this board is a 6 layer board with 2 power planes GND & VCC, we will first start with stub routing for the GND & VCC.

e. Select Whole Net Mode I, Auto route and select the GND signal at a pin location (repeat the same for VCC).

VCC

![](_page_56_Picture_8.jpeg)

. I	iteractive Move		
V /	Allow Component Move		
Γ	Minimum Force Indicator		
Е	Route Selection after Move		
Γ	Align Components		
E	Errors Allowed		
3	<ul> <li>Effort to Find Legal Position</li> </ul>		
☑ (	On Line DRC		
<u>ا ک</u>	Jse Working Grid		
e į	Dynamic Mincon		
(	OK Standard Cancel	Help	
	Push Aside		
	Dynamic pushing		
	Springback		
u	Push effort 4 💌		
	OK Cancel H	eln	

![](_page_56_Picture_10.jpeg)

![](_page_56_Picture_11.jpeg)

![](_page_57_Picture_0.jpeg)

The Place & Route Editor XR will help you in routing your designs by using several auto-routing technologies on a single net, a group of nets or within a certain area.

**Note**: By using the customizable *Function Keys F5 or F6* you can scroll through the layers from top to bottom or the other way around (Try it).

f. The next step is to create a Fan-out for a BGA. A Fan-out is a route template that can be applied to an SMD component. It enables routes to `breakout' from a surface mounted pad using a pattern that is efficient on space and gets the route to an inner layer as soon as possible. Fan-outs are often used and can be easily re-used for BGA's, QFP's or other devices.

![](_page_57_Picture_4.jpeg)

*Note:* If the Fan-out toolbar is not visible go to View→Toolbars→ select Fan out.

g. Before creating the actual Fan-out, select **Configure→ Routing Setup [Fan out]** tab - ensure the settings are equal to the example shown below.

Routing Setup	Pusher         Trunking         Composition         Fan-out         Testpoints         Radial         Spiral Vias         Autorouting Costs         Grids	×
Fan-out Process	1: 🔽 Simple Fan-out 2: 🗖 Autorouter Fan-out	
-Fan-out Settings-		
Simple Fan-out	Autorouter Fan-out	
Direction	Outwards  Via Position	
-Via Properties	First Length	
Gridded		
Via Name	Circle 20/10(via)	
Layer Pair	1 (Top Elec)	
California Marca	11 (Bottom Elec)	
Spiral vias	C Minimum Spacing	
	G Absolute First Length 0.700	
	C Incremental Second Length 0.700	
Description: Effort: 10	), Via: Cirde 20/10(via), Layer Pair: 1-11, Lengths: 0.700 0.700	
Open Sav	e As OK Cancel Help	

h. Select **Configure→Routing Setup [General tab]** and change the Width from Necked to Type and enter a value 0.152 mm.

**Note:** If your Units are set to *Thou*., as indicated at the bottom of the Place & Route Editor window, double click on the unit shown and change it to Millimeters with 3 decimals for precision.

![](_page_57_Picture_10.jpeg)

Select Routing→Fan-out→Perform Fanout <sup>3</sup> in the menu i. bar and click to frame an area around the component U4 (bga64) or just a number of pads.

Inwards

Outwards

If you would like to change the direction of the fanned out traces from Outwards to Inwards, select Configure→ Routing Setup [Fan-out] tab and change the direction from Outwards to Inwards.

Select the [OK] button on the menu and Undo the previous Fan out.

Select Routing -> Fan-out -> Perform Fan out 3/3 in the menu bar and click to frame an area around the component U4 (bga64) or just a number of pads. This time the pattern c\should be opposite.

When you are happy with the Fan-out you can save it for reuse, by selecting Routing→Fanj. out→Save IP (located on the Fan-out tool bar) and click to frame an area around the created Fan-out, so you can re-use it within other designs. Save the Fan-out as 'bga64.fpt'.

Let's test it!

Zoom-in on component U4 and Unroute 📐 the created Fan-out.

Select Configure -> Routing Setup [Fan-out] tab and change the direction to File. Click the file browse button and open the file **bga64.fpt** as shown on the next page.

Manual / Autorouting Pusher Trunking Composition Fan-out Fan-out Process 1: 🔽 Simple Fan-out Fan-out Settings Simple Fan-out | Autorouter Fan-out | Direction Outwards File Exit Inwards Via Properties Outwards Gridded NF E C SE Via Name 1 SW Laver Pai W 110 Disallow -

Spiral Vias

![](_page_58_Picture_10.jpeg)

(HTML Fan-out report dialog)

![](_page_58_Picture_11.jpeg)

![](_page_58_Picture_12.jpeg)

Manual / Autorouting Rusher	Trupking Compo	sition	Fan-out			
-Fan-out Process		Select F	Fanout Template File			
Tan out notess		00	🎉 🔸 Lightning_data 🖌 macros 🗸	👻 🚱 Sear	ch macros	
	1: I Simple Far	Organize	<ul> <li>New folder</li> </ul>			1 0
- Fan-out Settings			Name 🔺	Date modified	Туре	Size
			🌗 plot	8/3/2009 9:10 PM	File folder	
Simple Fan-out Autorou	ter Fan-out		퉬 wizards	8/3/2009 8:33 PM	File folder	
		<u> </u>	📄 bga64.fpt	6/23/2010 12:3	FPT File	
Direction File	<b>T</b>		Connector.fpt	9/2/2009 1:28 PM	FPT File	
	harman har C.A. Fab					
	/macros/bgao4.ipt	•				
-Via Properties						

Undo the previous fan out.

Select Routing-Fan-out-Perform Fan out 35 in the menu bar and click to frame an area around the component U4 (bga64) or just a number of pads. This time the pattern will come from the fan out file.

Tip: Once a design is fully "fanned out" the entire design can be saved to one fan out file. Each components' reference shapes' fanned out pin data will be saved. If the design ever needed to be rerouted using a different placement, the fan outs can easily be restored.

## Let's try another Direction

k. Select the Configure→Routing Setup [Fan-out] tab. Change the Direction to [Exit] and change the Via Position to Minimum Spacing as shown  $\rightarrow$ 

> Routing→Fan-out→Perform Select Fan out or click the icon 📑 located on the Fan-out tool bar and frame an area around the component U3.

![](_page_59_Picture_7.jpeg)

Routing Setup           Manual / Autorouting         Pusher         Trunking         Composition         Fan-out         Testpoints         Radial         Spiral Vias	?× (
Fan-out Process	
1: 🔽 Simple Fan-out 2: Г Autorouter Fan-out	
- Fan-out Settings	
Simple Fan-out Autorouter Fan-out	
Direction Exit	
SMD to Via Sparing	
Via Properties	
Via Name Circle 20/10(via)	
1 (Top Elec)	
11 (Bottom Elec)	
Spiral Vias Disallow	
C Incremental Second Length 0.700	
Description: Passes: 10, Effort: 10, Angle: 45, Errors Allowed: On, Pushing: On 🔽 Always Generate	to
Open Save As OK Cancel He	lp

This option uses the default pin exit directions for the various pad shapes as a guide to create the fan out entities.

This can be used on all SMD components to quickly and easily fan out an entire design. Try it!

![](_page_59_Picture_11.jpeg)

10

Routing Setup menu

For the next exercise open *Example3d.pcb* in the Design Editor and go to the P.R.Editor XR by selecting Tools→PR Editor XR 📓

The Place & Route Editor XR will help you to complete your design step-by-step by using advanced auto-route technologies. For instance; *Trunk Routing* will help you to complete data and address lines easier.

### What is Trunk Routing?

Trunk Routing introduces the concept of the intelligent trunk object, allowing you to route any given set of signals in an intuitive manner and with as little effort as possible.

BP I.

Selecting which connections are to be Trunk Routed

![](_page_60_Picture_6.jpeg)

![](_page_60_Figure_7.jpeg)

← Busses of data and address lines can be predesignated in a schematic design (as done in Example3.scm) and transferred to PCB and Place & Route Editor XR. A named bus (trunk) can be selected by its' bus marker.

Zoom in on the bus marker. Select **Manual Route** and (Shift + Click) on the round marker. This will start the action.

Alternatively you can double click on one of the  $\rightarrow$  pads as marked by the bus marker, before selecting **Manual Route**  $\boxed{\circleon}$ .

**Note:** All pads as marked will be selected and highlighted.

![](_page_60_Picture_12.jpeg)

![](_page_60_Figure_13.jpeg)

← When no bus marker is visible you can drag a multiple selection around a set of pins or connection wires before selecting **Manual Route** to start Trunk Routing.

![](_page_60_Picture_15.jpeg)

![](_page_61_Picture_0.jpeg)

Routing Setup	<u>? × </u>
Manual / Autorouting Pusher Trunking Composition Fan-out	Testpoints Radial Spiral Vias Autorouting Costs Grids
Automatic End Routing	Routing
Small Trunks	Automatically Minimize
Continuous More Than 2 Signals	Crossed-connections
Dynamic Ends Only     Continuous	
Dynamic Ends Only	Default Corner Style
	Use Routing Angle
	Box Via Pattern Style
Method: Method:	Allow Same Net Errors
Distance From Target: Distance From Target:	
Medium Medium	Width Change Style
	Use Routing Angle
Guides	Width
Active Snapping Single Click Finish On Snap Line	
Snap Distance Medium 🔽 Bus Marker Size Medium 💌	Necked Optimal
Snap Axis Length Medium	Optimal Intra-trunk Spacing
Description:	I ✓ Always Generate Auto
Open Save As	OK Cancel Help

#### n. Simple Manual Routing of a Trunk on a Single Layer

In order to aid routing, snap axes and trunk-end routing areas will be drawn on the canvas around each of the target sets of pins for the trunk. You will see *Twist Arrows* drawn on the canvas showing the best entry angle for the trunk to the target pins, this allows minimization of connections crossed at each end. You will also notice that you have a Gather Point for the trunk that is now dynamic on the end of your cursor. The Gather Point defines the start for the trunk where all of the parallel tracks will be considered as a single object.

To start routing the trunk you can place the Gather Point by clicking the left mouse button in the position that you want to start routing the trunk from. Trunk segments are now introduced towards the cursor position as you move the mouse on the canvas. Use the left mouse button to confirm trunk segments that you have added. A corner can be added by changing direction of movement of the cursor after a left mouse click.

**Note:** There are different styles of corners that can be added during trunk routing. This can be changed by using the Right Mouse Context Sensitive menu.

![](_page_61_Picture_7.jpeg)

![](_page_62_Picture_0.jpeg)

When you have added the required trunk path, it is possible to finish trunk routing in several ways:

- The **'Escape'** key can be used in order to finish trunk routing at the last added corner position or using the Right Mouse Context Sensitive menu **Cancel** option.
- With the 'Single Click Finish on Snap Line' option selected on the Trunking Options dialog, a single click when positioned over a snap axis will also finish the trunk. Remember to select Configure → Routing Setup →[Trunking] tab in the menu bar.

It is also possible to restart the Trunk Router on a previously added trunk. This can be easily done by selecting the manual routing icon and then picking the trunk on the canvas, or selecting the manual routing icon with the trunk item already selected **Note:** Try also the '*Backspace'* key (remove previous Item).

During routing of a trunk, the trunk contents will dynamically reorder to maintain the least number of crossed connections at each of the ends. This is done to give the best routing pattern for each end. This option can be configured using the *Trunking Options* dialog *Minimise Crossed Connection* setting.

### o. Adding Vias while Trunk Routing

To place a trunk via pattern while using the trunk router, you can double click the left mouse button or choose a different layer using the Layer option on the Right Mouse Context Sensitive menu. It is also possible to change the *trunk via pattern style* to a number of predefined styles using the Right Mouse Context Sensitive menu during trunk routing or by pressing the '*Tab*' key in order to cycle through the predefined trunk via patterns.

### p. Manual Reordering of Trunks and Via Patterns

It is possible to reorder the contents of a trunk manually, by manual selection of a single track inside the trunk using selection preview. Hold down the '**Shift**' key and press the Left mouse button. It is possible to switch to one of the other items by pressing the '**Tab**' key. Each time the '**Tab**' key is pressed the next item will be highlighted. You can then drag this track interactively to another position inside the trunk.

### q. Manual Trunk End Routing

You can use the Manual and Activ-45 routers to interactively route the connections up to the end of the trunk. During the routing process you can still re-order the trunk if necessary.

### r. Automatic Trunk End Routing

While you are trunk routing, it is possible to automatically route the ends of a trunk using the trunk end router. Routing will be attempted for all trunk ends that are inside a trunk end routing target area. Select **Configure**->Routing Setup->[Trunking] tab and ensure the settings are equal to the example shown below.

ZUKEN

louting Setup		?
Manual / Autorouting Pusher	Trunking Composition Fan-out	: Testpoints Radial Spiral Vias Autorouting Costs Grids
Automatic End Routing		Routing
-Small Trunks	Large Trunks	Automatically Minimize
Continuous	More Than 2 Signals	Crossed-connections
Dynamic Ends Only	Continuous	
	Dynamic Ends Only	Default Corner Style
		Use Routing Angle
		Via Pattern Style
Method:	Method:	Box
Use Routing Angle 💌	Use Routing Angle 💌	Allow Same Net Errors
Distance From Target:	Distance From Target:	
Medium	Medium	Width Change Style
-Guides		Use Routing Angle
Active Second	Cincle Click Einich On Sann Line	Width
Spap Distance Medium		G National C Contract
Snap Axis Length Medium		
scription:		Always Generate Auto
Open Save As		OK Cancel Help

In some circumstances you may wish to *decompose* trunk objects that you have added to your design into individual routes. For example, you may want to split a segment of a bus into routes so that you can route the bus around an obstacle. To do this, select the trunk items that you wish to decompose and then use the **Decompose** function on the Right Mouse Button menu.

![](_page_63_Figure_2.jpeg)

![](_page_63_Picture_3.jpeg)

**Note:** Once a trunk has been decomposed, it is not always possible to compose these items back into a trunk. If they have been modified beyond their closest spacings you can use the Trunk routing, manual and Activ-45 routers to interactively route the connections to the trunk end and finish the board.

If you didn't manage to complete the trunk routing then exit the P.R.Editor XR without saving and you will automatically return to the Design Editor and open *Example3e.pcb* 

### s. Auto Routing

For the next exercise you should open *Example3f.pcb* in the Design Editor and go to the P.R.Editor XR by selecting **Tools**→**PR Editor XR** 🖼

Before starting any auto routing I suggest you change the **[General] Routing Setup** options (CTRL-T). Setting them correctly is very important before any routing! Ensure the settings are the same as in the example shown.

Routing Setup	<u>? ×</u>
Manual / Autorouting Pusher Trunking Composition Fan-out Testpoints Radial Spiral Vias Autorouting Costs Grids	
Options Angle Track	_
Errors Allowed     45     Angled Autorouting     Straight     Style:     Curved	
Image: Second state       Image: Second	
Passes 10 I Enable Activ-45 Width: C Optimal	
Effort 10 Tidy Rectangle Size: 0.000 C Typed: 0.50800	
Via Fixed Items	-
✓ Vias Allowed     ✓ Respect Fixed Fan-outs	
Vias Under Single Layer Pads: Off  Use Maximum Length	
Enable Snap Vias Legal Distance: 0.000 Max Fan-out Length: 5.000	
Spiral Vias Disallow	
Post-Tool Tasks Equispace	
Auto Pour     Priority according to:	
Auto Teardrop     Change Length With Equispace     Completion     Auto Teardrop	
Freehand Number of Physical Errors	
Equispace Whilst Refine Routing	
Freehand Tidy     Use the best pass as the final autorouting result     Standa	- I
Description: 🔽 Always Generate Au	to
Open Save As OK Cancel He	p

*Note:* Although errors are allowed, you should first allow the router to make some errors. In combination with Effort 10 the router will continue routing till no errors are left.

![](_page_64_Picture_7.jpeg)

- *t.* Select **Routing** Autoroute from the menu bar and drag an area around the whole board outline or part of the board you would like to auto route. The auto router will stop automatically once all connections have been routed. The routing might not be optimal, and therefore you can run a Refine Routing Pass.
- u. Select Routing → Refine Routing ☐ from the menu bar and drag an area around the whole board outline or part of the board you would like to refine.

Note: As a result of the Refining Pass the number of vias and segments will be reduced.

If you didn't manage to complete the autorouting then exit the Place & Route Editor XR without saving, you will automatically return to the Design Editor where you can open *Example3g.pcb*, before going to the next step.

v. For the next exercise you should open *Example3g.pcb* in the Design Editor and go to the P.R.Editor XR by selecting **Tools**→**PREditor XR** 🖼

For test reasons you can decide to automatically generate a testpoint on every node (or as many as possible). Before starting any allocation of testpoints, select **Configure** $\rightarrow$ **Routing Setup** $\rightarrow$ [**Testpoints**] tab and ensure the settings are equal to the example. Do not forget to select '(Bottom Elec)' in the Layers section option!

Jsable	e Pads			Layers
	Use	Name	т <u>үр</u>	
1		Circle 20/10(via)	Via	
2		Circle 10(max)	Surface Mc	2 M 11 (Bottom Elec)
3		Circle 10(min)	Surface Mc	
4		Circle 47(max)	Surface Mc	
5		Circle 47(min)	Surface Mc	
6		Rectangle 1.3x1.2(min)@90000	Surface Mc	
7		Rectangle 24x74(max)	Surface Mc	
8		Rectangle 24x74(min)	Surface Mc	
9		Rectangle 74x24(max)	Surface Mc	
10		Rectangle 74x24(min)	Surface Mc	
11		bga64r(max)	Surface Mc	
12		bga64r(min)	Surface Mc	Pads for Added Testpoints
13		c0805r(max)	Surface Mc	Both Laverer
14		c0805r(min)	Surface Mc	
15		so 28x56r(min)@90000	Surface Mc	Top Layer:
16		Circle 40/20(via)	Through He	Bottom Layer: Circle 47(max)
17		Circle 55/28(via)	Through He	
18		Circle 60/32(via)	Through H	Separation
•	-			Center to Center Distance: 0.127

![](_page_65_Picture_7.jpeg)

![](_page_66_Picture_0.jpeg)

Now click on **Select** $\rightarrow$ **All** from the menu bar or you may use <Ctrl+A>, and all will be selected. Select **Routing** $\rightarrow$ **Testpoint** $\rightarrow$ **Allocate**  $\stackrel{\checkmark}{=}$  and the testpoints will be added automatically. Select **Utilities** $\rightarrow$ **Reports** $\rightarrow$ **Testpoints** to create a testpoint report as in the example.

Net		Туре	Layer	X Position	Y Position	Required Number	Testpoint Number	On Grid	Error	Near Pad	Requirement
	GND	(Via)	Bottom	107 442	75 311	1	Unused	Ves	> 0.000	114-60	Ver
	GND	(Via)	Bottom	100.855	70 485	1	Unused	Vac	> 0.000	C4-2	Voc
	GND	(Via)	Bottom	109.033	75 311	1	1	Yes	> 0.000	14-62	Yes
	AD7	(Via)	Bottom	67.310	61.595	1	Unused	Yes	> 0.000	U1-57	Yes
	AD7	(Via)	Bottom	83,439	61.595	1	Unused	Yes	> 0.000	112-2	Yes
	AD7	(Via)	Bottom	101,981	61.595	1	1	Yes	> 0.000	U3-2	Yes
	AD6	(Via)	Bottom	86.741	60.833	1	Unused	Yes	> 0.000	U2-3	Yes
	AD6	(Via)	Bottom	101.981	60.833	1	Unused	Yes	> 0.000	U3-3	Yes
	AD6	(Via)	Bottom	67.818	60.071	1	1	Yes	> 0.000	U1-56	Yes
	AD5	(Via)	Bottom	68.326	59.055	1	Unused	Yes	> 0.000	U1-55	Yes
•	4D5	(Via)	Rottom	101 081	58 470	1	Unusad	Vac	> 0 000	112-4	Va
Re	port		Lock							Close	Help

Now that you have finished the design, you can select **File Exit** from the menu bar and rebuild the results. If you didn't manage to finish the testpoint creation, just open **Example3h.pcb** to see the finished results.

RIF Import Options	×
Import RIF Changes only	Do NOT Reconnect
🔽 <u>G</u> roup Trunks	
💌 Eix Grouped Trunks	
Show this dialog on return from well as through File Import/Op	m PREditor XR (HS) as otions
Cancel	<u>H</u> elp

![](_page_66_Picture_5.jpeg)

![](_page_67_Picture_0.jpeg)

# Step 4 - Manufacturing Data for Design C

If you like, you can create the manufacturing data for this design by just selecting **File** $\rightarrow$ **Manufacturing Export** $\rightarrow$ **Batch Process**  $\checkmark$  in the menu bar. In the Batch Process window select [Open]  $\rightarrow$ *Manufacturing Output 6 Layer.ppf*, which you can find in the Self teach directory and click [*START*].

**WELL DONE!** You have now completed the PCB design and experienced several features of the advanced Standalone Place & Route Editor XR2000.

Check CADSTAR Place & Route Editor XR - Functionality Matrix on:

**ROUTING MATRIX** 

![](_page_67_Picture_6.jpeg)

![](_page_68_Figure_0.jpeg)

• Chapter 5 - Design D (Single Sided Board Design)

![](_page_68_Figure_2.jpeg)

Transistor Audio Amp (50mW)

# Information on Design D - Transistor Audio Amplifier

Design D is based on the same schematics as Design B (a little audio amplifier). But this time you will create a SINGLE SIDED board and I will show you how to add jumpers on the fly. Typically, a jumper is used to bridge across other routes, the jumpers discussed here are *non-functional* jumpers and do not appear in the schematics. I will guide you through it to give you some tips. The sequence is the same as before.

# Step 1 - Design D

a. Open *Example2.scm* and transfer the schematic to PCB through **File→Transfer to PCB**..., but now choose '*1 layer 1.6mm.pcb*' as PCB technology instead. This is a default technology file that I have already prepared for you; notice that although I'm using the same library, the solder-pads are larger, there are thicker track-widths and more spacing has been defined.

# Step 2 - PCB Placement for Design D

You can now start to place and arrange the components on the PCB after the transfer. Again, I will give you some important points to follow in order to complete the PCB placement or you can go immediately to *Step 2.i.* 

When creating a single board design a good placement is highly important to avoid crosses in the connections, so take your time. Don't worry as you will be able in Place & Route Editor XR to add jumpers on the fly, just like adding a via.

![](_page_68_Picture_11.jpeg)

b. Change in the shape toolbar the Default Shape Type to Board

![](_page_68_Picture_13.jpeg)

×

![](_page_69_Picture_0.jpeg)

- c. Draw a board outline (size 2000x1500 thou). If you didn't manage to draw the board outline, just open *Example4a.pcb*
- 🔜 d. Arrange components around the Board Outline 💷
  - e. Manually place the critical components inside the board outline: Place VCC9V at X-position 150,0 and Y-position to 150,0 Place INPUTGND at X-position 150,0 and Y-position to 1050,0 Place INPUT at X-position 150,0 and Y-position to 1350,0 Place SPK at X-position 1850,0 and Y-position to 1350,0 Place SPKGND at X-position 1850,0 and Y-position to 1050,0
  - f. Fix the position of VCC9V, INPUTGND, INPUT, SPK and SPKGND
  - h. Cross-probe if it is necessary
- i. Automatically place the other components. If you didn't manage to place the components, just open *Example4b.pcb* 
  - j. Before going to the routing environment check out **Settings→ Defaults→General** and ensure Jumper support is enabled.

Defaults	X
Jumper Suppor	t
Test Lands <u>C</u> ode:       Circle 60/32         Documentation       ▼         Layer:       Documentation         ▼       Pads/Vias         Drill Oversize:       0.000         Thermal Relief       Clearance:         0.254       Relief Width:	Components Mirror Design Options Jumper Support Enabled Suppress Inner Layer Pads Legacy Constraint Management Idy Connections By Option By Item
	OK Cancel Help

![](_page_69_Picture_9.jpeg)

k. Also before going to the routing environment check out Libraries→PCB Components II. If you expand the contents of the PCB.LIB (as shown below) you will see a sub folder for Jumpers. I have already created some pre-defined jumpers, which you will be able to select in Place & Route Editor XR on the fly.

💼 Library Manager		×
Current Library		
Path: C:\Users\Public\Zuken\(	CADSTAR Express 13.0\Library\	•
Type: PCB Components		
File Name: pcb.lib	Brow	se Create
Add Folder Rer	ame Folder Delete Folder << Log	ate
Edit ⊡® pcb.lib	JUMPERNF-lead0.8 (1016)	🔲 Use Mapping file
Properties	JUMPERNF-lead0.8 (1270)	Add File
Temporary	JUMPERNF-lead0.8 (1524)	
Delete		
Archive	SUMPERNE-(1603 (reflow IPC)	Save Lomp
	JUMPERNF-r0805 (reflow IPC)	Iidy Library
Report	JUMPERNF-r1206 (reflow_IPC)	
<u>O</u> rigins		Assignments
⊻ersions		User Attributes
		Layers
Select All		
C Show subfolder contents	0 Selected From 8 Listed	Un <u>i</u> ts
Show selected folder only	<u>C</u> lose	

I. Open *Example4b.pcb* and go to the Place & Route Editor XR2000 by selecting **Tools→PREditor XR**... 🖾

![](_page_70_Picture_3.jpeg)

## Step 3 - PCB Routing for Design D

You are now at the final stages of the PCB design. Simply follow the steps and you will complete your PCB design very soon. When transferring to the Standalone Place & Route Editor XR a *RIF Export Option* window will be showed automatically. Ensure that *Write Jumpers from Library* is **enabled**.

![](_page_71_Picture_2.jpeg)

a. Before starting any routing I advise you to check the Routing **Setup** options. Select **Configure** →Routing Setup [General] tab in the menu bar (or use CTRL-T). Ensure the settings are equal to the example. If you don't like copper to be poured automatically disable it. If you don't like routes to be pushed you can disable the *Pusher* or reduce the *Effort* in which case less routes will be pushed aside.

Manual / Autorouting Pusher Trunking Composition Fan-out Testpoints Radial Spiral Vias Autorouting Costs Grids
Options Angle Track
J Errors Allowed     45     ✓ Angled Autorouting     Style:       ✓ Allow Pin Swaps     C Curved
I On-line DRC
Passes 10  Enable Activ-45 Width: Optimal
Effort     10     Image: Tidy Rectangle Size:     0.000     C     Typed:     0.50800
Via Fixed Items
Vias Allowed
Enable Snap Vias Legal Distance: 0,000     Max Fan-out Length: 5,000
Spiral Vias Disallow
Post-Tool Tasks Equispace 🔽 Save Best Pass
Auto Pour      Priority according to:
Auto Teardrop
Freehand
Enable Freehand     Carling Control to the final autorouting result
Standard
Description: ayer Pad: Circle 47(max), Top Layer Pad: , Both Layer Pad: Circle 20/10(via), Center to Center Distance: 0.127 🔽 Always Generate
Open Save As OK Cancel Help

![](_page_71_Picture_5.jpeg)


**Tip:** By using the customizable *Function Keys F5 or F6* you can scroll through the layers from top to bottom or the other way around. Select in the menu bar *Layer*, change the Current Layer to *Bottom Elec* and click *OK*.

Layer Settings											
		Preset:		•	On	Off					
		Layer	Current	Active	Display	Bias					
		1 (Top Jumper)	0			Jumper					
		2 (Top Elec)	0			Y bias					
		4 (Bottom Elec)	$\odot$			X bias					
	5 (Bottom Ju		0	•		Jumper					
				-	-						
		ОК	Ap	ply	Close	e Help					

Note: 2 layers have been added to this technology (Top Jumper and Bottom Jumper)!

b. Manually route 1.1.1.1. the net between resistor R2 and capacitor C2 as in the example on the Bottom Elec layer.



In the next step you will add a jumper on the fly by manually routing **LILL** the net between transistor TR1 and resistor R2 as shown in the example below on the Bottom Elec layer.

c. Route to the location you want to add the first pad of the jumper and double click, select *Top Jumper*. Now move the cursor to the location you want to add the second pad of the jumper. P.R.Editor XR will show you a thin line representing the pitch of the pre-defined jumpers depending on the available space. Double click again and you will add the jumper and you can continue routing. P.R.Editor XR will show you only a list of pre-defined jumpers if more than one jumpers with the same pitch have been defined in the library. It's as easy as adding a via!

Select	
1 (Top Jumper) •2 (Top Elec) 5 (Bottom Jumper)	
ОК	Cancel





Now route all the connection on Bottom Elec layer and insert jumpers if necessarily till no connections are left.

d. Once you have finished the design you can select **File**→**Exit** from the menu bar. All routing and jumpers will be back annotated to the PCB Design. Running an ECO update won't remove jumpers and the jumpers will appear normally in the Part List and placement data.

If you didn't manage to complete the design, just open *Example4c.pcb* to have a look.



#### Design D after Placement & Routing





# Step 4 - Manufacturing Data for Design D

At this stage, you can also create the manufacturing data (Gerber, N.C.Drill, Parts List, Placement data etc.) for the manufacturing of the PCB (as you did for Design A) by selecting **File→Manufacturing Export→Batch Process** ... in the menu bar. In the Batch Process window you select [**Open**] and use *Manufacturing Output 2 Layer.ppf*, which you can find in the User directory and click [**START**].

d B	Batch Process - [C:\Users\Public\Zuken\CADSTAR Express 13.0\Self					
		Use	Description	Variant	Process Type	
1			Gerber Copper pattern Component	<no th="" va<=""><th>Artwork</th></no>	Artwork	
2		•	Gerber Copper pattern Solderside	<no th="" va<=""><th>Artwork</th></no>	Artwork	
3		◄	Gerber Solderresist Componentsid	<no th="" va<=""><th>Artwork</th></no>	Artwork	
4		$\mathbf{\nabla}$	Gerber Solderresist Solderside	<no th="" va<=""><th>Artwork</th></no>	Artwork	
5		$\mathbf{\nabla}$	Gerber Silkscreen Componentside	<no th="" va<=""><th>Artwork</th></no>	Artwork	
6			PDF Assembly Componentside	<no th="" va<=""><th>Artwork</th></no>	Artwork	
7			Partlisting	<no th="" va<=""><th>Report</th></no>	Report	
8		<u>&lt;</u>	Placementdata	<no th="" va<=""><th>Report</th></no>	Report	
9		•	Drilldata (Plated Through Holes)	<no th="" va<=""><th>N.C. Dri</th></no>	N.C. Dri	
10	)	•	Drilldata (Non-Plated Through Hole	<no th="" va<=""><th>N.C. Dri</th></no>	N.C. Dri	
11	I	~	PDF Drill Drawaing	<no td="" va<=""><td>Artwork</td></no>	Artwork	

You can easily *disable* the rows that you do not wish to post-process. In this design, since it is a *single layer board*, the layers that are to be generated are *Bottom Elec, Top Solder Mask, Bottom Solder Mask and Top Silkscreen* (all in Extended Gerber RS274-X format). Other additional manufacturing data that CADSTAR can generate which is necessary for manufacturing are *Parts Lists, Placement Data and Drill Data*. All manufacturing data will be saved in the *Output* directory.



Alternatively you might want to produce an **ODB++** output file. ODB++ is one of the most intelligent CAD/CAM data exchange formats available today, capturing all CAD/EDA, assembly and PCB fabrication knowledge in one single, unified database.

# WELL DONE! You have now completed the PCB design.



### Chapter 6 - Design E (Reusing Circuits to build a Double sided Board Design)

The exercises that you have done so far are fairly easy, but they still take time to create. It is always good to save circuits for *Reuse* at a later date.

In this chapter you are going to build a design that uses two completed design circuits into one board. In Chapter 1, if you saved your circuit as a Reuse Block you are on your way. If not, they are available for you to use

Reuse Blocks are stored in the ..\**Reuse Files\** folder. However they can be stored and read from Network Locations. See **Tools →Options →[File Locations] tab**.

Options	×
System File Locations Library Paths Interaction Display Constraints Cross Probing Reports Tools Macros Debug	
File types Location:	
Colour Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\Colours\         Initial Design Directory       C:\Users\Public\Zuken\CADSTAR Express 13.0\Self Teach\         Macros       C:\Users\Public\Zuken\CADSTAR Express 13.0\Nacros\         Manufacturing Output       C:\Users\Public\Zuken\CADSTAR Express 13.0\User\         Output Datasheet Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\User\         Output Report Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\User\         Reuse Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\User\         Selection Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\Self Teas\         Simulation Libraries       C:\Users\Public\Zuken\CADSTAR Express 13.0\User\         Selection Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\Self Teas\         Selection Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\Self Teas\         Selection Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\Self Teas\         Selection Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\Selections\         Simulation Libraries       C:\Users\Public\Zuken\CADSTAR Express 13.0\Selections\         User Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\Selections\         User Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\Selections\         User Files       C:\Users\Public\Zuken\CADSTAR Express 13.0\User\         User Files	
C:\Users\Public\Zuken\CADSTAR Express 13.0\Reuse Files\ <u>M</u> odify	
OK Cancel <u>H</u> elp	

**Tip:** It is recommend that for each reusable schematic circuit that is stored away, the corresponding PCB Circuit be saved in the same location and by the same name. In the CADSTAR Express install tree "../Reuse files/" you will find **Flasher.SCM** and **Flasher.PCB** as well as **Amplifier.SCM** and **Amplifier.PCB**.

- a. Open the sample file Exercise5a.SCM. This file has a sectioned off area for each circuit. However, If you want to create your own new schematic design you may do so.
- **b.** Add the "Flasher" Reuse circuit to the new sheet. Select [**Actions**-Reuse blocks-Insert Reuse Block]
  - c. Select the Flasher circuit and click [OK]
  - d. Place the circuit into the Flasher area on the sheet.
  - e. Repeat the process for the Amplifier circuit.

That's it for the Schematic!





- f. Run [Transfer to PCB] and select PCB Technology Exercise5\_2 Layer pcb.
- g. During the Schematic Collating process, you will be prompted to [Add New Code] or [Choose Existing Code] until you are presented with a report. For this example simply select [Add New Code] and [Yes] for all options.



**Note:** That during this process the schematic design assignments are being compared to the Design Assignments that are in the Template files. Adding them is important unless you are choosing from the existing assignments.

h. Review the report and then click [Close].

Your new PCB design will display all components in the lower left corner of the window.



- i. Open the Workspace, Current Design window and expand the list of Reuse Blocks and you will see Amplifier and Flasher as shown above.
- j. Click the Flasher circuit and then click the [Move] tool bar icon to move the Flasher components out of the pile away from Zero, Zero.



- k. Repeat for the Amplifier Components.
- I. Click the Flasher circuit and then click the [R.M.B] to *Update the Reuse Block.*

#### Read the Notes below before proceeding.

You will now be presented with the opportunity to map the layers that are used in the reuse PCB blocks to the Layer stack-up of the new design.

If the Circuit was designed on a 2 layer board and you are importing it onto a 4 layer board then you may use the [Choose Existing Layer] option and select the correct layer until all are properly mapped.



You will also be presented with options to choose how to handle matching Signal names. I.e. If GND is used in one block and DGND is used in another you could always address that with a Starpoint component. However if GND is used in both blocks it is possible that each ground is supporting a higher voltage potential and should not be joined, In that case choose the option to [Rename Net]

The remaining options should always be reviewed since they pertain to Pad Code and Route Width code assignments from the Reuse Blocks. To properly maintain the integrity of the block(s) you should typically select the [Add New Code] option for all of the selections.

- m. Place the **Flasher** block on the lower half of the PCB Design and attempt to align the Mounting Holes with those on the new PC board shape
- n. Repeat Steps 'l' and 'm' for the Amplifier block and place it on the upper half of the PCB board shape.

From this point forward with real designs, you would complete the necessary steps to finish any Interconnect routing between the blocks that may have resulted from the *Joined Nets* and use the **Embedded Place and Route Editor** to re-pour the copper templates.





WELL DONE! You have now completed a PCB design using Reusable Circuit Blocks!



For more information visit www.zuken.com/cadstar



### Conclusion

After these six exercises you should now be more familiar with the basics of PCB design. In the near future you may even be designing a more complex PCB using CADSTAR.

With this booklet, you have received a free copy of CADSTAR Express. CADSTAR Express provides a number of features of the full CADSTAR version, only limited by the number of components (max 50) and pads (max 300).

For further information on pricing or if you require any support during evaluation or prefer to receive a detailed demonstration, please contact your local CADSTAR distributor:

http://www.zuken.com/products/cadstar/where-to-buy.aspx

There are also other CADSTAR tools that help Schematic and PCB designers to create board layouts.

## Check for more information on CADSTAR products:

### http://www.zuken.com/cadstar

I hope to see you again when we talk about some of our other, more advanced products:



# See you soon!



For more information visit www.zuken.com/cadstar