Application Notes

A Potentially Significant On-Wafer High-Frequency Measurement Calibration Error

■ James C. Rautio and Robert Groves

High accuracy radio-frequency (RF) measurements typically require a calibration to remove the undesired effects of the measurement apparatus. The calibration consists of measuring some combination of known standards such as short, open, load, through, and delay. When measurements are performed on-wafer for silicon RF integrated circuits (RFICs), a two-step calibration/de-embedding technique is typically used. First, the measurement system is calibrated to a reference plane located at the probe tips through measurement of calibration standards fabricated on an impedance-standard substrate. Second, on-wafer de-embedding standards are measured in an attempt to shift the reference plane to the terminals of the device under test (DUT). While significant effort has gone into the development of improved on-wafer de-embedding schemes, discrepancies between actual and de-embedded data still exist.

In this article, we first discuss a specific case (a spiral inductor on silicon) for which there was a significant discrepancy between measurement and analysis. The problem is found to be with the measurement. This problem is detailed, and a technique we call "synthetic calibration" is described that can be used with any electromagnetic (EM) analysis to quantify calibration error for any proposed set of calibration standards. Due to the high expense and time required for wafer fabrication, it is important to successfully complete such a calibration validation prior to tape-out.

The Problem

Figure 1 illustrates the spiral inductor including the ground-signal-ground-signal-ground (GSGSG) feed structure. As is common in Si RFICs, there is no ground plane on the underside of the substrate. For this feed structure, the three ground pads are connected together by a strip that is in ohmic contact with the conducting silicon substrate. The problem described in this article can also occur when two GSG probes are used (as is much more common) to measure a two-port with input and output ports on opposite sides of the circuit, and when coplanar-like ground strips (i.e., a "ground cage") are used, even when an insulating substrate is used.

The inductor was analyzed using a planar EM analysis and then fabricated and measured. The EM analysis models metal thickness with multiple sheets as shown. Current on the side of thick metal can vary sharply from top to bottom, with the strongest current at the sharp corners at the top and bottom. In addition, the side current penetrates the metal due to skin depth. When this penetration is on the order of or larger than the gap between lines, allowing skin-depth current to penetrate into the sides can be important. Modeling thickness with multiple horizontal sheets includes both effects. When these effects are important, modeling the side current with a single, vertical, infinitely thin sheet should be avoided.

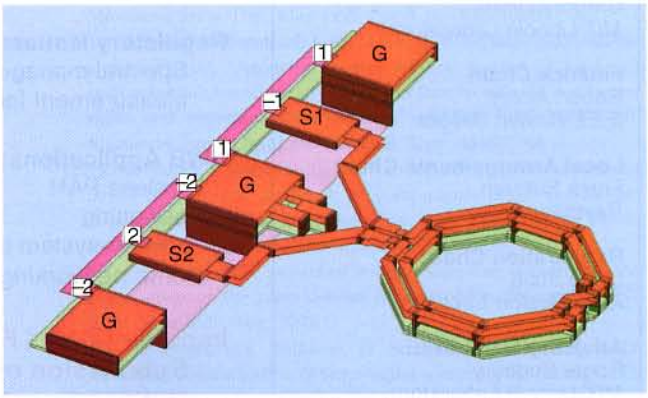

Figure 1. *A spiral inductor on silicon including the GSGSG probe pads. The inductor is intended to operate as a differential inductor, however it is measured as a two port. Metal thickness is modeled with multiple sheets (vertical dimension magnified for clarity in all figures).*

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The difference between measured and calculated inductance (not shown) is considered insignificant. The difference between measured and calculated Q is also considered insignificant below 3 GHz (see Figure 2). However, above 3 GHz, the differences become design critical.

Whenever there is significant (as determined by design requirements) difference between measured and EM calculated results, we typically first consider the possibility that the analysis is in error. Also, note that in Figure 2, the analysis predicts a higher Q than is measured. For a worst case, we usually assume that the result from the EM analysis is optimistic and that the measurement is correct. Supporting this conclusion is the fact that two other EM analyses (not shown) predict Q that shows better agreement with the measured result, only a little lower than was measured. With measurement and two additional EM analyses all essentially agreeing, our job is to figure out what went wrong with the illustrated EM analysis result.

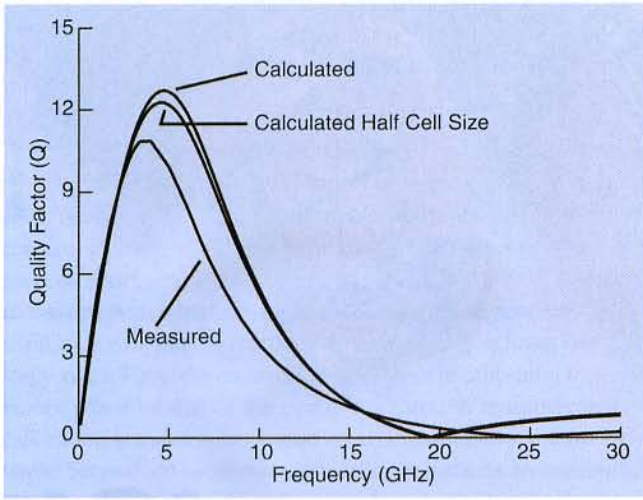

Figure 2. *The EM analysis shows significantly higher Q than measured. Repeating the EM analysis with half the cell size shows little change.*

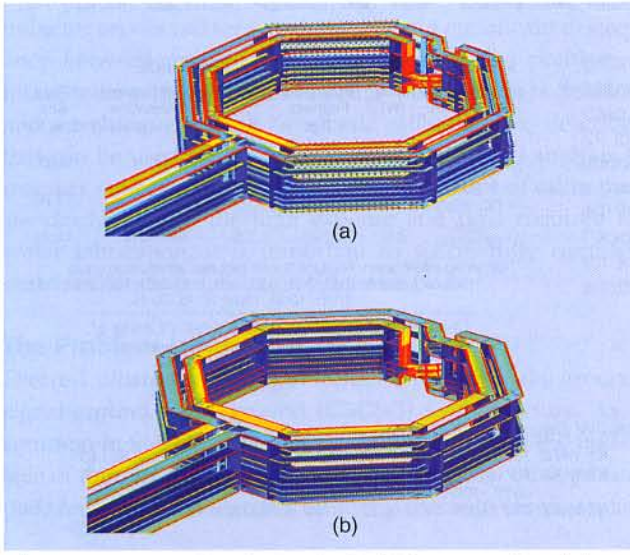

Figure 3. *Current distribution (red is high current, blue is low current) using the original cell size (a) shows strong high edge current, critical for accurate analysis of loss. With the cell size cut in half (b), we see even better representation of the edge current.*

Analysis Error Evaluation

Fortunately, it is easy to rapidly run numerous numerical experiments to test possible sources of error. The first thing to do, whenever any kind of numerical EM results are suspect, is to view the current distribution, especially when loss is important. Large errors in current distribution result in small errors in S-parameters. However, small errors in S-parameters result in large errors in loss. If loss is important, you must have an accurate current distribution.

The correct current distribution has high current on all conductor edges and is smooth everywhere. The high edge current is particularly important because any time current is constricted, loss increases. Error in representing the high edge current directly contributes to error in analysis of loss. In order to correctly include loss due to high edge current, EM analyses must have "edge meshing" turned on. In some EM analyses, this is the default, while in others it must be manually invoked. When loss is important, the designer must be absolutely certain that edge meshing is used.

In Figure 3(a), we see the current distribution for this inductor. Because this current distribution is the result of a numerical EM analysis, it is at best only an approximation of the actual, exact, current distribution. To be certain that the analysis is accurate to within design requirements, we must quantify the analysis error.

With EM analysis, the approximate magnitude of the error is easily determined. Simply remesh the entire circuit at half the cell size. Figure 3(b) suggests that the high edge current is indeed more accurately represented. Figure 2 shows that the resulting change in Q is insufficient to explain the observed difference between measured and calculated results.

In Figure 3 (and in all the other figures), the vertical dimension is magnified to allow close inspection of the thickness model. We can see that the current on the edges of each sheet varies depending on their location in the thickness stack. The total metal thickness is only a few microns, illustrating that very fine meshing vertically, no matter what EM analysis is used, is needed to accurately model thickness.

Notice also that skin depth on the sides of the thick lines is easily modeled with the multisheet model. Figure 3 is the current distribution at 30 GHz. There is little current on the interior of the metal lines deeper than the skin depth. The current distribution at low frequency flows equally on all sheets, including in the interior, due to the very large skin depth.

For this problem, we considered many possible sources of error. For example, the analysis used here includes the effect of a perfectly conducting box enclosing the circuit. A possible error source is the inductor ground return current flowing through the lossless box sidewalls rather than through the substrate. Analysis with a much larger box realizes almost no change in the calculated Q; the box is not the error source.

After exhaustively eliminating numerous possible analysis error sources, we are forced to consider measurement error.

Measurement Error Evaluation

In considering the possibility of measurement error, we are once more faced with numerous hypotheses. The line of investigation that proves fruitful starts with, "Where does the ground return current flow?"

The answer is not obvious. Let's consider a simple equivalent circuit for this spiral inductor (see Figure 4). The inductor and its metal resistance are represented by the series resistor and inductor. The capacitors are the capacitance between the inductor and the silicon substrate. The shunt resistors are the resistance of the silicon substrate.

This inductor is designed to be driven with a differential excitation. In this case, the current on Port 1 equals minus the current on Port 2. Ground-return current flows under the inductor as indicated by the central arrow in Figure 4. In this case, the current to the port ground terminals is zero.

However, this differential inductor is measured as a two-port with any two-port excitation/termination possible, and, in general, the ground-return current for each port is nonzero. This current flow is indicated by the right and left arrows in Figure 4.

Figure 5 shows this ground-return current path in the measured inductor, as viewed from underneath. The substrate resistance is split into two resistors: one for resistance under the inductor and the other for resistance under the feed structure. We should include the resistance under the inductor in the measurement. The resistance under the feed structure must be removed by the calibration; it is not part of the inductor.

Figure 6 shows the short calibration standard used in the measurement. Its ground-return current is indicated with an arrow. Notice that the short circuit does not include the substrate resistance under the feed structure. In fact, the entire substrate resistance under the feed structure is completely unknown to the on-wafer calibration. There is no way that the calibration can remove this substrate resistance.

This substrate resistance is in series with the inductor's capacitance to the substrate. This means that the substrate resistance is expected to have little effect at low frequency where the capacitance has a large reactance. In Figure 2, we see that Q error is insignificant at low frequency.

Figure 7 shows the EM analysis structure (used to obtain the EM data in Figure 2). In this case, the feed structure is a very long pair of lines. The substrate ground return resistance is very large, but it is all removed by the EM analysis de-embedding. Except for well-understood and rare failure mechanisms, the EM de-embedding is exact to within the accuracy of the underlying EM analysis. Figure 7 shows the de-embedding reference plane for the EM analysis with lumped components illustrating the ground return path. The resistance under the feed structure has been removed.

While a faulty calibration standard that fails to remove the feed structure substrate resistance appears to be a good explanation of the problem, we must still test it quantitatively.

Substrate Resistance Hypothesis

We can test the substrate-resistance hypothesis by evaluating the resistance of a perfect short circuit. This seeming contradiction (a "perfect" short that has resistance!) is formed from the spiral inductor of Figure 1. The inductor is removed from the layout, and a perfectly conducing wall is placed at the desired reference plane. The ground-return current must now flow from the sidewall through the substrate and back to the ground terminals of the GSGSG probes. EM analysis combined with PI net synthesis yields a value of 53 Ω for this resistance over a broad band.

Thus, if we add 53 Ω of resistance to the ground terminal of the EM analysis of the spiral inductor (easily done with any circuit theory based analysis), we should see a Q that is close to the measured value, and, indeed, we do (Figure 8). There are still differences due to the fact that our modification to include the effect of the substrate resistance under the feed structure is not exact and because, in this analysis, we have included only the on-wafer portion of the complete feed structure; we can not exactly reconstruct the defective measurement.

An important warning is best noted at this time. The substrate conductivity of silicon is sometimes not known with high accuracy. Thus, there is a strong temptation, when data like that of Figure 2 is presented, to modify the substrate conductivity in the analysis until the measured and calculated data match exactly. In this case, the intentionally introduced error in the analysis substrate conductivity exactly compensates for the

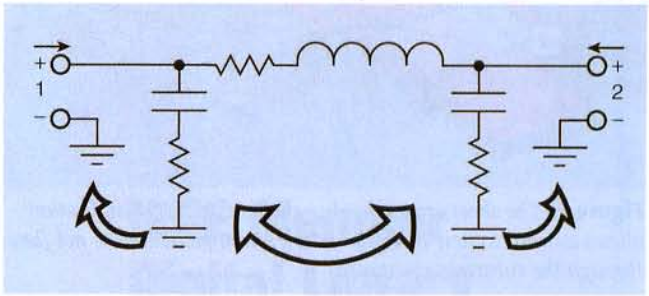

Figure 4. *A simple equivalent circuit for the spiral inductor shows ground return current (arrows) flowing through resistors that represent the silicon substrate. This schematic illustrates double-ended, not differential, operation.*

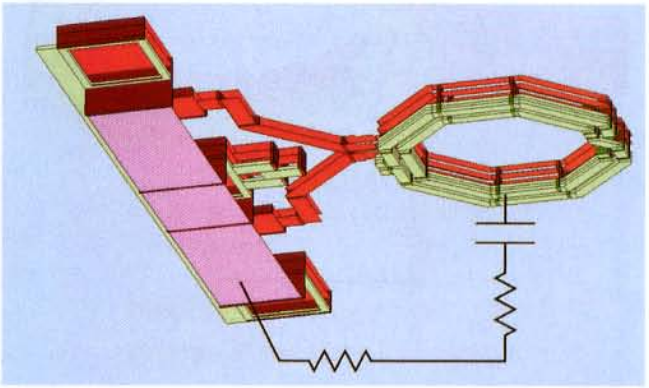

Figure 5. *The inductor ground return current flows from the underside of the inductor to the ground pads in the feed structure as shown by the superimposed circuit components. The resistance under the feed structure is not part of the inductor.*

error due to improper measurement calibration. If this kind of "tuning" of analysis parameters to match measurement is done, the faulty measurement remains hidden. This situation must be avoided at all cost.

Exact agreement between measured and calculated maximum Q should also be carefully investigated. Notice that in Figure 2, maximum Q is very sensitive to the EM cell (or mesh) size. As the mesh is refined (i.e., the cell size is repeatedly cut in half), the result for maximum Q should converge uniformly to the measured value. However, an extremely fine, and typically impractical, mesh size is required in order to achieve visually identical results. If visually identical results are seen, one should consider performing a convergence analysis (i.e., refining the mesh) to make sure that the EM analysis results are actually going to continue converging *past* the measured result.

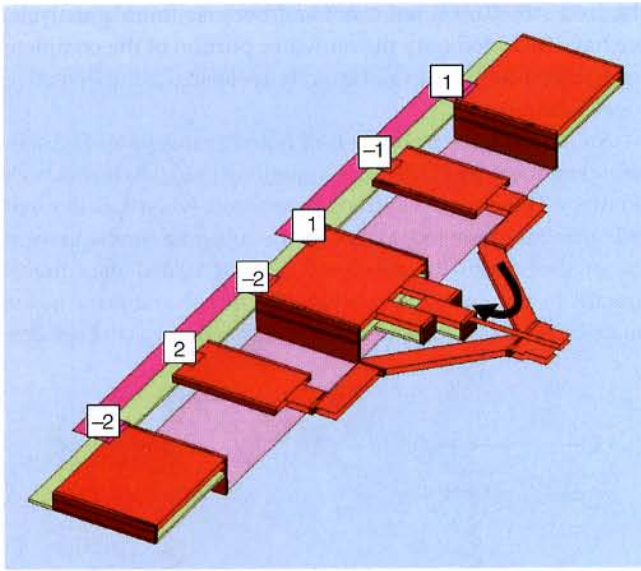

Figure 6. *The short circuit used in the measurement calibration allows current to flow directly to the ground pads. It does not flow through the substrate resistance.*

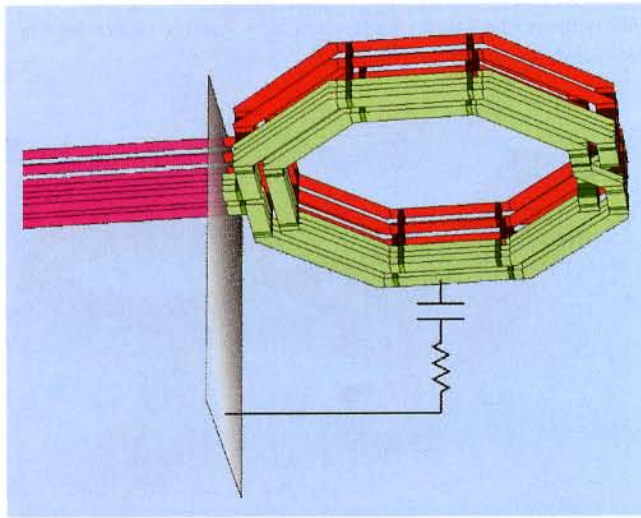

Figure 7. *The feed structure used by the EM analysis consists of two very long lines. The considerable ground return resistance is removed by the EM de-embedding algorithm, setting the reference plane as indicated.*

Note that a commonly used short-circuit standard is a simple patch of conductor shorting the probe pads upon which probe tips are placed. There is absolutely no ground current flowing in the substrate for such a short circuit. In contrast, if the DUT has any ground-return current flowing in the substrate, the measured loss in the DUT can be significantly and incorrectly degraded.

Figure 9 shows the tangential E-field on the surface of the silicon substrate. This is exactly proportional to the current flowing in the surface of the silicon substrate. Notice that the current strongly concentrates directly under the conductors forming the spiral. This can act as a guide to forming an effective ground screen to increase Q.

Insulating Substrates

This measurement problem also occurs with insulating substrates, where the two substrate resistances of Figure 5 become capacitors and the associated conduction currents become displacement currents. If there is no substrate resistance, and we define Q (as it is calculated throughout this article) to be the negative of $\text{imag}(Y_{11})/\text{real}(Y_{11})$, then the Q of a spiral inductor is

$$Q = \frac{\omega L - (\omega^2 L^2 + R^2)\omega C}{R},$$

where L = inductance, R = series resistance in inductor, and C = shunt capacitance from one side of the inductor to ground.

Notice that as the capacitance increases, the Q decreases. With an insulating substrate, the shunt capacitance to ground is greatest for the EM analysis reference plane as shown in Figure 7 (with the resistor becoming a capacitor). The perfect ground of the EM reference plane is close to the underside of the inductor, maximizing the shunt capacitance to ground.

For measurement, the shunt capacitance develops from the underside of the inductor to the ground pads of the GSGSG probe pads (see Figure 5), with both resistors becoming capacitors. This is a much farther distance; thus, the shunt capacitance is smaller. This means the erroneous measurement yields a Q higher than that predicted by the EM analysis.

Thus, when this measurement error is present, measurement of Q on insulating substrates is higher than the EM analysis result, while exactly the opposite is true for highly conducting substrates. This leads us to conclude that, for a given feed structure, for some value of substrate conductivity, the erroneous measurement can yield a correct value of Q.

This is not good news; this means a measured versus calculated plot of Q can appear to give good agreement while the complete measurement is substantially in error. This measurement error also has little effect on inductance. Thus, comparison of inductance and Q is insufficient to determine whether or not success has been realized. Additional comparisons are absolutely required if certainty is desired. For

example, comparing the real and imaginary parts of Y_{11} and Y_{22} is very sensitive to this measurement error.

Recommendations

A wafer fabrication is a huge investment in time and effort. Because of this, we strongly recommend that when accurate on-wafer measurements are required, on-wafer standards be used to calibrate all measurements and that the necessarily nonideal on-wafer standards be quantitatively evaluated for the measurement error that they introduce. This can be done by means of synthetic calibration and measurement.

For a synthetic calibration, nothing is built; all standards and DUT S-parameters are the result of the EM analysis. The calibration is performed using exactly the same de-embedding software as the physical measurement, except all input data comes from EM analysis. To evaluate the expected measurement error, simply compare the results of the synthetic measurement of the DUT to the normal EM analysis result of the same DUT. Differences between the two indicate the approximate magnitude of the expected measurement error. Keep in mind, as described in the previous section, that comparing only inductance and Q is insufficient.

One should, of course, be certain that the EM analysis de-embedding can achieve high accuracy as well. One example test is to simply de-embed a through line or a coupled line to zero length. Other simple but sensitive tests are easily devised.

Failure to perform a synthetic calibration places the entire wafer fabrication in needless jeopardy. The total investment in time to perform a high accuracy synthetic calibration is about one day of computer time and one hour of engineering time.

The error mechanism described in this article is invoked when the ground-return current for the short-circuit calibration standard is different from the ground-return current for the DUT. This can be the case when two GSG probes are used to measure a two-port (as in the common case of input and output ports being placed on opposite sides of the circuit), when coplanar wave (CPW)-like ground strips are used, when the substrate includes a bottom-side ground plane, and even for circuits on insulating substrates. To reduce the significance of this error mechanism, design the short circuit so as to reduce the difference between the short circuit and DUT ground-return current paths. To quantify the error, perform a synthetic calibration. Even if a "trusted" and well established on-wafer calibration procedure is used, it can be advantageous to know the realistic range of measurement error that can be expected so that any future increased accuracy requirements can be quantitatively compared to actual measurement capabilities.

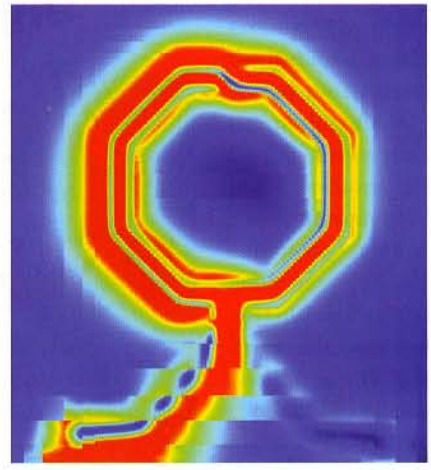

Figure 9. *Current on the surface of the silicon is concentrated under the spiral conductor turns. This suggests the proper location for a loss-reducing ground screen.*

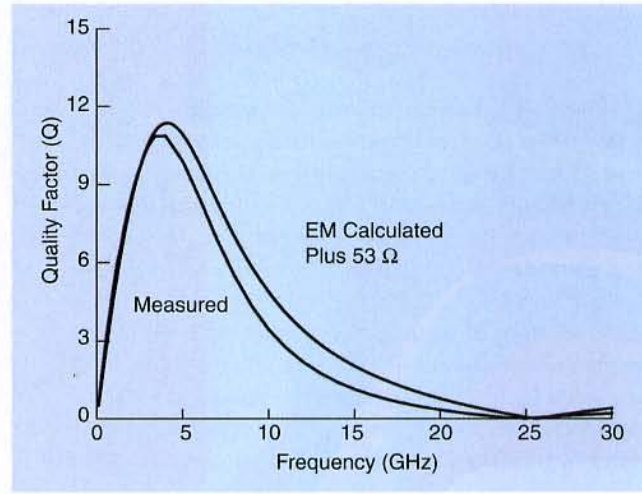

Figure 8. *The measured Q compared to the original EM analysis data modified to include the substrate resistance under the feed structure shows significantly improved agreement.*

When using industry standard open/short on-wafer de-embedding to shift the measurement reference plane from the probe tips to the terminals of the DUT, this measurement de-embedding problem cannot be completely avoided. More complex de-embedding methodologies must be investigated that can take into account the ground return current that flows in the substrate between the DUT and the probe pads.

As we have seen above, the results of a measurement can depend significantly on the ground-return current path. Another example of where this can be a problem is when components are measured within a ground cage (wide, low-loss conductors surrounding the DUT that connect ground pads of GSG probes), but are later used in circuits lacking the ground cage. All the current that flows in the ground cage during initial measurement is forced to flow through the resistive substrate when used in an actual design. Large errors are likely to result.

Conclusion

A previously unrecognized and possibly common on-wafer calibration error has been discovered and explored. This error reduces the measured Q of the spiral inductor on silicon when a high conductivity substrate is used. The measurement error incorrectly increases the Q for insulating substrates. A "synthetic calibration" is introduced and is used to quantify this, and any other, measurement error due to nonideal on-wafer standards prior to wafer fabrication. This reduces the risk that measurements from a wafer fabrication will be rendered useless by measurement error.