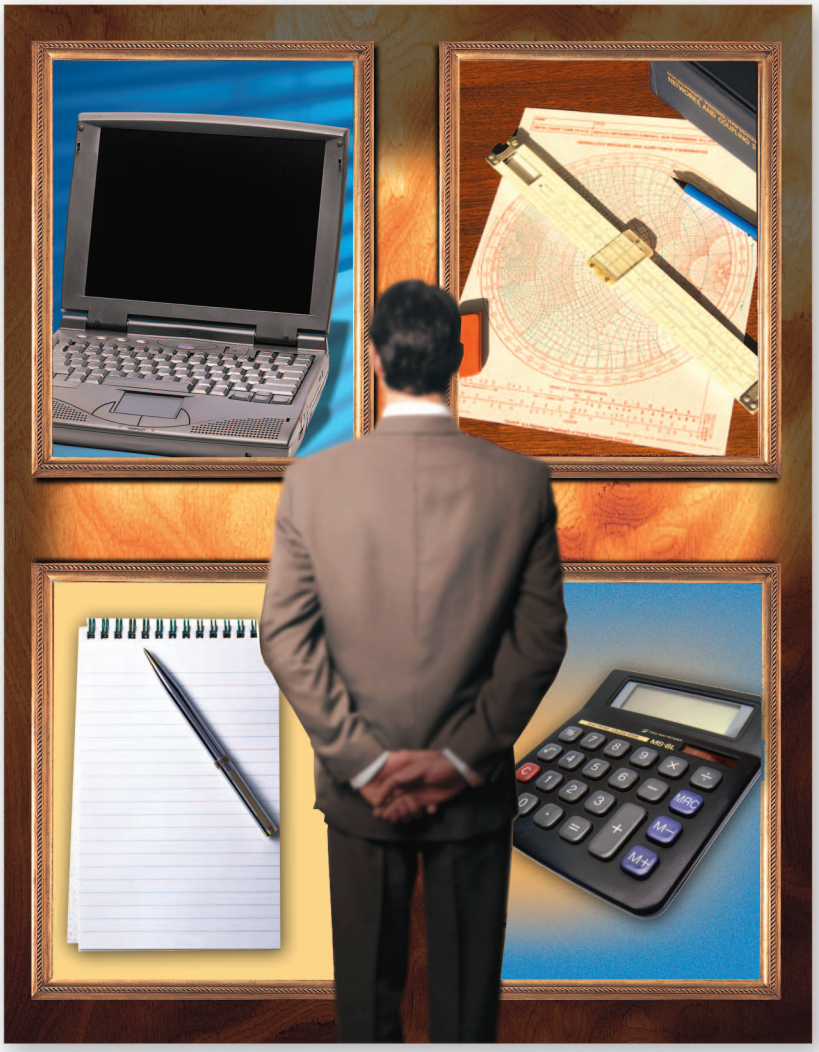
EM-Component-Based Design of Planar Circuits

James C. Rautio

When I first started doing microwave design, the pocket calculator was just starting to replace the slide rule and the Smith chart was king (Figure 1). After a few years, I moved on to developing electromagnetic (EM) software using the brand new personal computer. That is where I have been ever since. Over that time, I've seen EM software progress from "useless academic ivory tower junk" (as I was actually told by a skilled microwave engineer) to becoming a critical part of nearly every microwave and high-frequency design today.

Over the last several years, I have been on the road almost six months out of each year visiting microwave design houses and universities all over the world. In the early days, designers used EM software simply to verify a design once it was complete. Today, I find that most designers use either a tuning methodology, a companion modeling methodology, or some combination of the two to tune the final design with EM analysis. (If you are not using one of these techniques—or worse yet, if you are using direct EM optimization—you need to change, and quickly.)

Today, we are on the verge of yet another major change in the way we use EM software. This change stems directly from a seemingly minor and esoteric subject—internal EM port calibration. In this article, I start with a quick tutorial about the ports used in EM analysis and how they are calibrated. Then, I discuss a new development—perfect internal port calibration. Finally, I conclude with a few examples illustrating the impact that perfect internal port calibration will have on microwave design.



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EM Wave Ports

When I learned microwaves at Cornell in the mid-1970s under Prof. G. Conrad Dalman, we used slotted line (in rectangular waveguide) to make measurements. To calibrate, we slapped a flat piece of metal, a perfect short circuit, across the end of the waveguide. Prof. Dalman said that that was our "short-circuit reference plane."

Today, I find that most designers use either a tuning methodology, a companion modeling methodology, or some combination of the two to tune the final design with EM analysis.

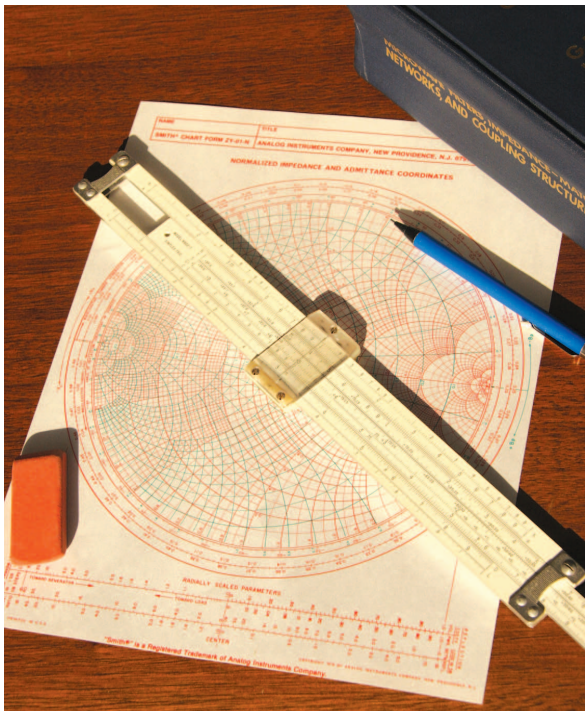

Figure 1. *The Smith chart and slide rule were the primary microwave design tools in the 1970s and before.*

Then we would slide the detector along the slot in the rectangular waveguide and measure the actual standing wave inside the waveguide. Next, we removed the short and attached the device under test (DUT) to the waveguide and precisely measured how the standing wave changed. That, combined with exact knowledge of the characteristic impedance of the single propagating mode in the waveguide, allowed us to calculate the reflection coefficient of the DUT. We had just performed a calibrated measurement of S_{11}.

One type of port in modern EM analysis is sometimes called a wave port. A wave port can be excited by a previously calculated modal distribution. It can also be excited by a transmission line that is long enough that all higher-order evanescent modes are gone. The EM analysis looks for the standing wave and then calculates the *S*-parameter, just like Prof. Dalman taught us.

The problem is in calculating Z_0, the characteristic impedance of the line. For a rectangular waveguide, we calculate Z_0 essentially exactly. However, for inhomogeneous media, like microstrip, Z_0 is no longer unique. Depending on which definition of Z_0 we use (voltage-current, voltage-power, or current-power), a 10% variation is easily seen. A 10% error in Z_0 means 10% error in the result. Sometimes this Z_0 problem is put in terms of defining a line integral from the transmission line conductor to ground to calculate the line voltage. Same problem, different name.

The fundamental constraint is that when we excite a circuit, the excitation itself introduces error into the result. While the amount of error is not terribly significant for a lot of work, it completely precludes conducting exact port calibration. And why would anyone want an exact calibration anyway? What we are doing right now works just fine, right? Play along for a little bit and let's see.

EM Gap Ports

EM researchers call them "infinitesimal gap excitation" or sometimes "magnetic frill excitation." The concept is simple. Imagine a microstrip line. To excite the circuit, take a razor knife and cut a narrow gap in the line. Now imagine a tiny voltage source. Connect the two terminals of that voltage source across the gap. We call this a "gap port." What is neat about gap ports is that the gap voltage is unique. It is the voltage across the infinitesimal gap. There is only one answer for the gap voltage. Likewise, the port current is unique. If you assign, say, 1.0 V to your voltage source and run the EM analysis, there will be only one value for the current flowing out of that voltage source. Thus, the port current/voltage (i.e., the port input admittance) is unique.

I use these gap ports exclusively. My work is with shielded EM analysis of planar circuits [1], [2]. The shield is a perfectly conducting box surrounding the circuit. We place the gap in the microstrip line so that it separates the end of the microstrip line from the box wall (Figure 2). Then one terminal of the voltage source is connected to the perfectly conducting box wall and the other is connected to the microstrip line across the infinitesimal gap. This excites the circuit, current flows, and we can calculate the unique input admittance of the circuit.

However, even when we have the unique input admittance, the problem is not yet solved. Just like wave ports, gap ports introduce error into the result. If we want an exact port calibration (for whatever reason), we must exactly characterize and remove that error.

Exact Gap Port Calibration

Box wall ports are gap ports located on the edge of the circuit right next to the shielding box wall. I solved the exact box wall port calibration (also known as "deembedding") problem for shielded analysis back in 1991 [3]. A more recent summary, including extension to unshielded analysis (with limitations) and generalization to any arbitrary port discontinuity, is presented in [4].

Known as double delay [the more general version is known as short open calibration (SOC)], it works just like, and was inspired by, modern network analyzer calibration. Several standards are analyzed and the port discontinuity is characterized and removed from the analysis. The double delay uses two through lines, one double the length of the other (Figure 3).

An advantage for shielded analysis is that the port discontinuity is always a pure shunt capacitance; there is no series inductance. The more general SOC technique works for any port discontinuity and also works for unshielded EM analysis. However, it is limited when inductance/capacitance in the port discontinuity starts to look like the transmission line to which it is connected, and it fails when there is radiation. Thus, shielded analysis is preferred for this approach.

If you dig into the math of double delay and SOC, you see another advantage of using this kind of calibration with a shielded analysis. It turns out that the perfectly conducting sidewalls of the shielding box are effectively used as perfect short-circuit reference planes. Wow…just like the short-circuit reference planes Prof. Dalman used on the rectangular waveguide! We shall see that these perfect short-circuit reference planes are also critical in achieving perfect calibration of internal ports as well.

This type of gap port calibration makes no use of any guesses as to what the Z_0 of the port connecting line may be. Thus, it does not suffer from ambiguity in what definition of Z_0 to use. A nice benefit of this approach is that after we calibrate a length of transmission line, we can look at the result and figure out what Z_0 would give us the same *S*-parameters we got from the EM analysis. We call this the transverse electromagnetic (TEM) equivalent Z_0 [5]. This is the one and only Z_0 that you must use in any circuit theory program to get the same current/voltage relationship at the ports as you got in the (perfectly calibrated) EM analysis. So, instead of suffering the Z_0 ambiguity problem, gap port calibration actually solves the Z_0 problem!

The U.S. motto is "In God We Trust." As scientists and engineers, we add to that, "All others must have proof." Since I am a mere human and you are a good engineer, when I claim that double delay is exact, you will first ask what I mean by "exact" and then you will say, "Oh yeah? Well prove it!" Fair enough.

"Exact" refers only to the calibration; any and all error in the underlying EM analysis remains in the data. Further, exact means to within numerical precision provided the assumptions of the calibration are met. Yup, the "assumptions" are the fine print, and the fine print is important. Pay close attention: We assume that the port connecting lines are not overmoded. If you have one signal conductor, there is only one propagating mode. If you have two coupled lines, there are only two (even and odd, perhaps) propagating modes,

Box wall ports are gap ports located on the edge of the circuit right next to the shielding box wall.

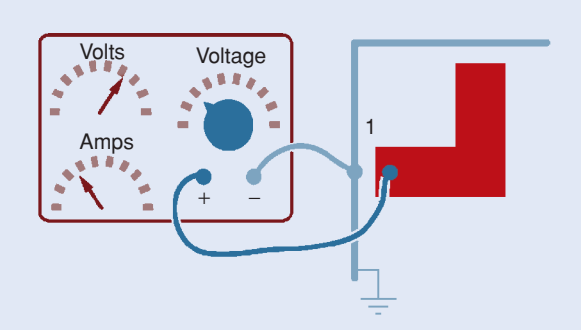

Figure 2. *The gap port is a voltage source impressed across an infinitesimal gap. In this case, the ground terminal of the voltage source is connected to the perfectly conducting sidewall of the shielding box that contains the circuit. This is called a box wall port.*

etc. This is a pretty reasonable assumption as operating overmoded is usually a fatal design error.

There are several subtle ways a line can be overmoded. For example, in grounded coplanar waveguide (CPW), a microstrip mode (between the signal line and ground plane) can be excited. If your CPW ground returns are not symmetrical, you can excite a slot line mode. In some circuits, radiation can unexpectedly deliver power from input to output, resulting in failure (another reason this type of calibration is best applied to shielded EM analysis). As long as you are aware of and watch for these failure mechanisms, you can use this type of port calibration safely. And because most of these calibration failure modes also result in design failure, you are also more likely to build a circuit that actually works as well.

Another failure mode is to select a calibration length, *L* (Figure 3), that is too short. In this case, even the evanescent modes (i.e., the fringing fields around the ports) transfer power from input to output, yielding the same bad result as an overmoded line. Be sure to keep *L* longer than one or two times the width of the line. To check for this, or any of the above failure modes, compare the results of two analyses, each done with a different value of *L*. A good answer is independent of *L*.

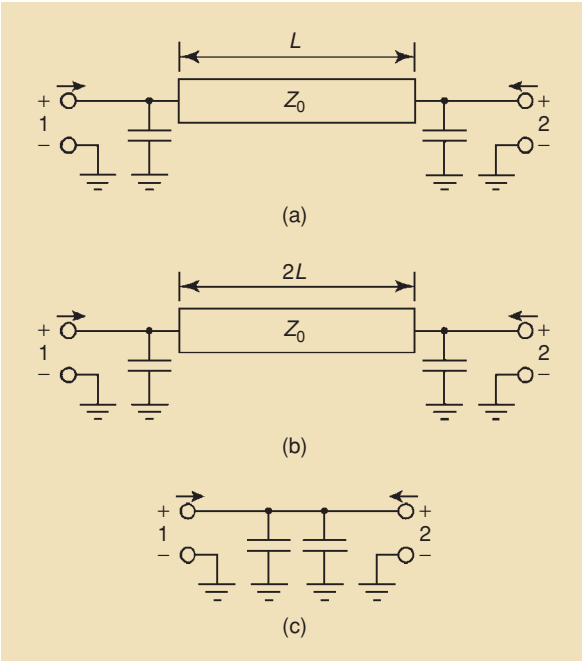

Figure 3. *The double-delay EM port calibration algorithm uses two delay lines, labeled a and b, one double the length of the other. With this information, the port discontinuity (the capacitor) can be exactly determined and removed as desired. (Figure reprinted from [4].)*

Typically, the above failure modes are rare. However, as an engineer, failure mechanisms are interesting to explore, and we do just that with several examples below.

So, how do we prove this amazing claim of exactness? One way is to show asymptotic convergence to the exact answer [6]. Another way is to take a filter and split it in two (Figure 4). Fortunately, this process is automated. Just draw the line and analyze. The filter is automatically split into two pieces; each piece is analyzed and automatically reconnected. Figure 4 shows the result. The EM analysis of the entire filter and the reconnected analyses of the two half-filters exactly overlay each other. If there were any error in the port calibration, the split-up/reconnected filter response would be wiped out. By the way, splitting a large circuit into smaller pieces like this is a great way to get faster analysis. This particular filter can even be split into four or five or more pieces if desired.

Internal Port Calibration

Internal ports are ports that are not on the edge of a circuit. Such ports might be used, for example, to mount surface-mount devices (SMDs). They might also be used for transistors in integrated circuits. The problem is that in most EM analyses, internal ports are not calibrated at all. Even in my own EM analysis, such internal ports were only partially calibrated.

Figure 5 shows one way to do internal ports. Each number indicates a gap port with a voltage source

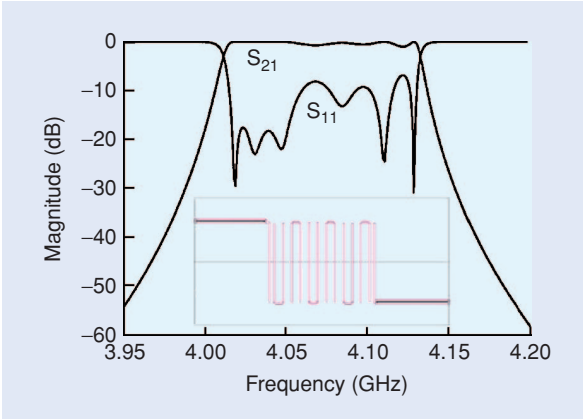

Figure 4. *To demonstrate exactness of the port calibration, a hairpin filter is split in two as indicated by the horizontal line in the inset image. The two half-circuits are created, analyzed, and then attached together (all automatically) to give results that can not be visually differentiated from the analysis of the entire filter.*

impressed across it. Notice that ports on the left and top sides have minus signs in front of the port numbers. This reverses the "+" and "−" terminals of the voltage sources. The central patch is the ground for all the ports. We must have the "−" terminal of each voltage source connected to ground. The via from the patch to the bottom of the box attaches this local ground patch to the global box ground. Thus, even these local internal ports have the same ground reference as the box wall ports.

Well, at least at dc. Now for the problems. At high frequency, the via has inductance. This places the local ground at a different potential from the global ground. In addition, the patch itself has inductance, meaning each port on the patch has a slightly different ground potential. This is in addition to all the self and mutual capacitances of and between all the gap ports. Nasty situation.

Fortunately, the capacitances and inductances are usually small, so we just ignored them for many years. We could still get pretty good results. Most of the time. Every now and then, we would get a report of a problem that could not be handled. Then the reports started coming a little more frequently as designers were pushing limits. Then we got a report of a problem from a very major customer. Okay, time to solve the problem.

So, I went into immersion. When I do that, it is literally nothing but eat, sleep, and work the problem. I did this for 30 days, the longest immersion I have ever done. There were a lot of surprises I never expected, but the problem was solved, and the solution is now completely published [7]. (It seems we are unique in this aspect. Most, if not all, other commercial EM calibration algorithms are kept as trade secrets for some reason.)

Top level, very simply, we treat the local ground of Figure 5 as a DUT. We then analyze and de-embed the

local ground using our exact box wall port calibration. This sets our short-circuit reference plane (remember what Prof. Dalman taught us!) exactly at the edge of the local ground. Once the local ground is exactly characterized, we mathematically and exactly remove it and substitute a perfect ground reference for all internal ports. Thus, this is a two-tier calibration. The first tier exactly characterizes the imperfect local ground. The second tier then exactly removes the effect of the imperfect local ground.

I keep mentioning these short-circuit reference planes for good reason. If you want high accuracy, the short-circuit reference planes for the component that you insert into the calibrated ports must be at the exact same location as the reference planes for the calibrated ports. This is true for both EM-analyzed components and for models you might get from a component vendor. Take SMD components, for example. Some vendors are precise about where the reference plane for their model data is, what substrate it was measured on, what size mounting pads were used, etc. You have to know and decide whether, for example, the mounting pads are in your component data or in your EM analysis. If the pads are in both sets of data, you include them twice. If they are in neither set of data, you don't include them at all. Don't take chances. Know precisely what you are doing.

For terminology, we call this calibration a "general local ground (GLG) calibration" (or deembedding). In my EM software, we call the ports that use this calibration algorithm "cocalibrated ports."

For what, every good engineer will ask, would we ever need this so-called exact calibration? And once more, what do you mean by "exact," and can you prove it? Wait a moment for the first question. The second question is answered next.

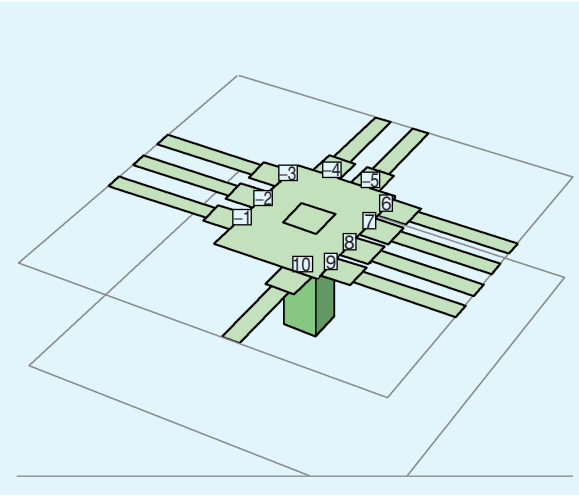

Figure 5. *Internal ports set up to accept an SMD with the via to global ground providing a global ground reference. The sign on the port numbers indicates which terminal of the voltage source is ground.*

GLG calibration of internal ports has the same limits as the first-tier double-delay calibration for box wall ports.

Cocalibrated Port Validation

Validation is actually a side result of what we do in this section. Our main objective is to break the calibration in order to determine its limits. Then we have a good idea of where and when we can use it, and then we can decide if it is actually going to be useful.

GLG calibration of internal ports has the same limits as the first-tier double-delay calibration for box wall ports. It is exact to within numerical precision provided the assumptions are met. The main assumption is that the port-connecting lines are not overmoded. Sound familiar?

Basically, the lines connecting the local ground to the box walls (Figure 5) can not be overmoded, they cannot be too short, and they can not be radiating (that is why this technique is not so useful for unshielded EM analysis).

Let's get really tough now. We want to break things. So we make our first validation example a microstrip line on very thick silicon. The line is 1-μm thick copper (5.8×10^7 S/m), 12 μm wide on top of 4-uM SiO_2, on top of 800 μm of silicon, conductivity 1.0 S/m. I have often found that the easiest way to stress an EM analysis is to analyze on a thick, conducting substrate.

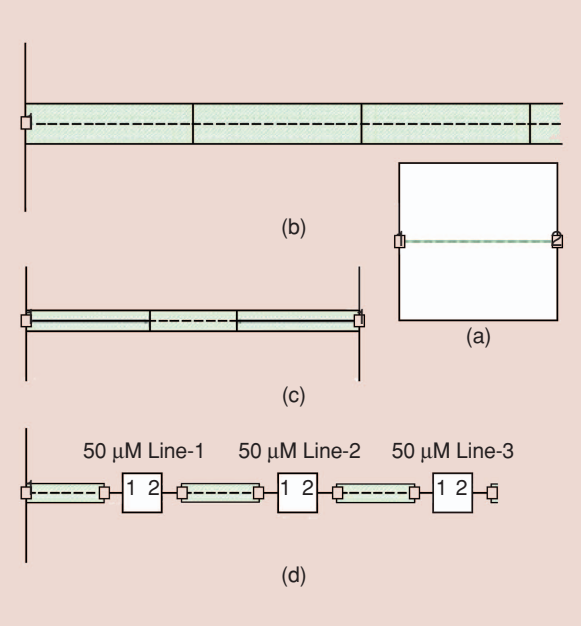

Figure 6. *The first validation structure (a) is a $1,000 \times 12$ μm line on silicon cut into 50-μm segments, as detailed in (b). The test structure has every other 50-μm segment replaced with a pair of cocalibrated ports (d). The S-parameters of a 50-μm line (c) are then connected into the ports.*

Another way to stress the internal port calibration is to use lots of internal ports. The line in Figure 6 is drawn as a cascade of 50-μm long rectangles for a total length of 1,000 μm. This is our baseline structure. For the test structure, we remove every other 50-μm length of line and substitute a pair of cocalibrated ports. After the EM analysis, the S-parameters of a separately analyzed 50-μm length of line are inserted into each pair of cocalibrated ports. This is done automatically by an internal nodal analysis. We call the inserted 50-μm length of line a "component." If the calibration is indeed exact, then we should get the same answer for both the baseline structure and the test structure.

Another big mistake is to measure a circuit component in CPW and then use it in microstrip in the final design.

Note that we only remove polygons from the baseline structure to create the test structure. The EM meshing is based on the polygons. If we change a polygon as we create the test structure, the meshing would change. If the test structure mesh is different from the baseline, then we can no longer expect the test and baseline structures to give exactly the same answer, even if the internal port calibration is exact.

It's Broke!

Figure 7 shows the results. Notice that we have a substantial difference between test and baseline above about 20 or 30 GHz. Something went wrong; we broke this so-called exact calibration. Remember the assumptions? I wonder if we have some kind of multimode propagation, even though this is a simple microstrip line.

Or is it so simple? A microstrip line has current going out on the signal line and returning on the ground plane. Hold on here! Where's the ground plane? There is a ground plane on the bottom of the shielding box, 800 μm below the signal conductor. But, there is also conducting silicon 4 μm below the signal conductor. Which one gets the return current? Perhaps both do!

One way to check this hypothesis is to use a shorter calibration length L (Figure 3) in the first-tier calibration. The default value of L is on the order of the size of the box—1,000 μm. This is kind of big. So we change the calibration length to 90 μm, the ground return current will certainly flow through the 90 μm of resistive silicon rather than down one 800-μm box wall and up the other. When we plot test versus baseline, the sets of curves are now visually identical, strongly supporting our hypothesis. (The curves are so exactly one on top of the other, it is pointless to actually present the plot here.)

Let's be paranoid (this is good for engineering survival). Did we make the calibration standard too short? Good question, and easy to test. Reduce the calibration length to 40 μm. The results are still visually identical. Values of calibration length between a few hundred down to 20 μm or so work well for this circuit. Of course, shorter calibration lengths analyze faster.

Controlling Ground Return Current

To further test the multiple ground return current hypothesis, I returned to the default (long) calibration standard lengths that failed so dramatically in Figures 6 and 7. But now, I am using two strips (Figure 8). I provide my own ground return in the form of the second strip. Note that the additional ports are −1 and −2. This means that for every 1 A of current that flows into port 1, exactly 1 A of current is forced to flow out of port −1. Now, by Kirchoff's law, the current in the box wall (coming from the silicon and the box bottom) is zero. The microstrip mode is open circuited at the ports and we have slot line! The silicon is not the ground return and the box bottom is not the ground return. All ground return current is along the second strip.

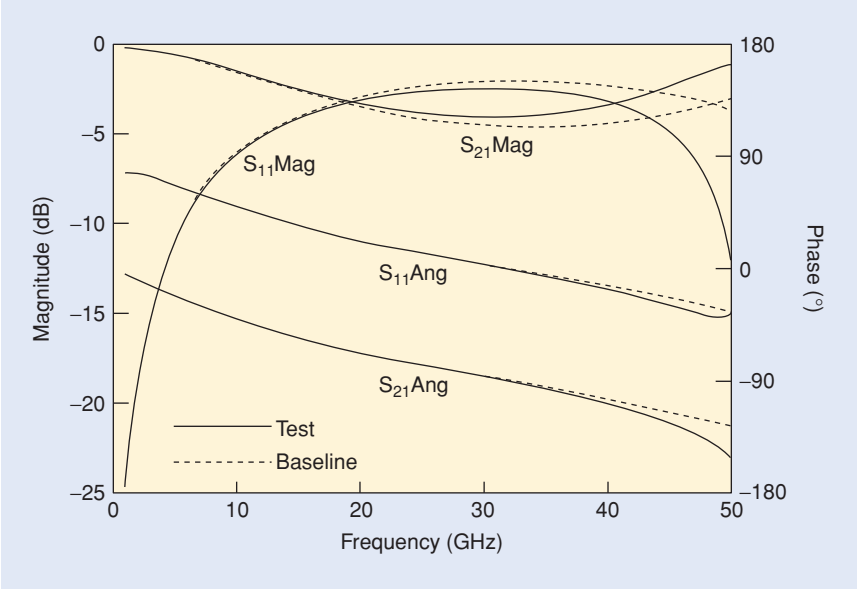

Figure 7. *We see substantial difference between the baseline structure and the test structure above 20–30 GHz. This appears to be due to multiple ground return paths. Specifying shorter calibration standard lengths solves the problem.*

The 50-μm long lines that I insert into the cocalibrated ports of the test structure are now four-port lines; each 50-μm long line has its own ground return. When I perform this analysis, we now obtain visually identical results. It looks like the multiple ground return paths can be a problem.

This problem actually highlights a potential fatal design flaw in using microstrip on silicon at high frequency. Depending on how big your circuit is, and how you excite it and mount it, you could get this same multiple ground return situation. This could result in ground loops, radiation, substrate coupling, etc. Basically, electrons simply do not care what we decide to call ground. In any RF circuit, you must always and forever have a complete circuit, and that includes the ground return. If the loop formed by your complete circuit is large, it will radiate and couple and do all kinds of nasty things. Putting a ground return right by the signal line, especially at these kinds of frequencies is a very good idea.

Also popular is coplanar waveguide (CPW). This simply includes a second ground strip on the other side of the signal line (ports now numbered −1, 1, and −1). This is very common, but also dangerous if not carefully used. As mentioned above, if the ground return currents are not symmetrical (equal in both ground strips), then in addition to your CPW mode, you also have one or more slot line modes—multimode propagation. This will not affect the calibration because the calibration standards are always symmetrical. But it could affect the response of your circuit. Be careful.

The GLG calibration exactly removes all the self and mutual inductances and capacitances between all the cocalibrated ports in each group.

Another big mistake is to measure a circuit component (like an inductor) in CPW and then use it in microstrip (leaving out the CPW ground strips) in the final design. People actually do that! Incredible!

Do I Really Need Internal Port Calibration?

The answer is, "very possibly not." For example, if you have no need for the types of EM design methodologies that use internal ports, you certainly don't need calibrated internal ports. What if you use internal ports without calibration? Figure 9 shows what happens when the GLG calibration is not used for the example

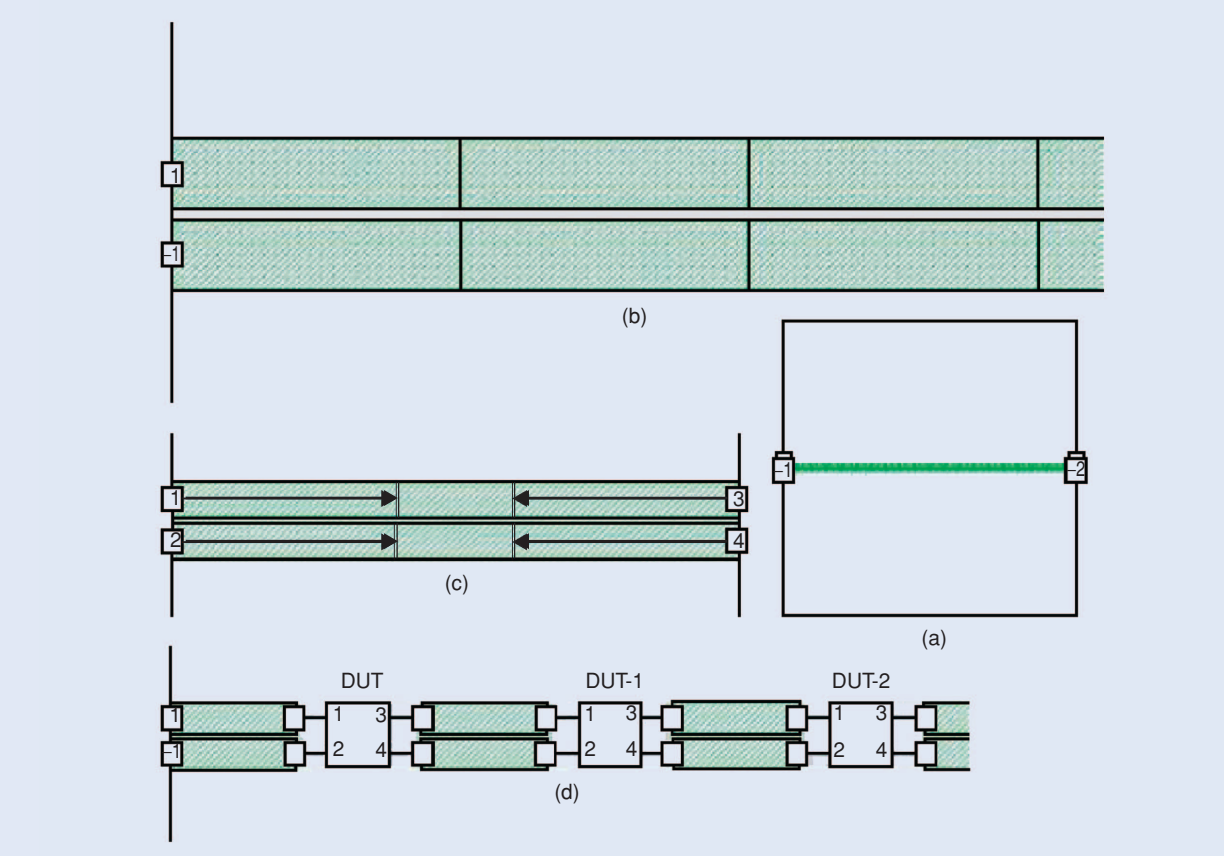

Figure 8. *The multiple ground return problem is also solved by including an explicit low-impedance ground return (between the negative port numbers). Baseline structure is (a) with detail (b). The 50-μm long lines (c) that are inserted into the test structure (d) are now four ports because they too include their own ground return strips.*

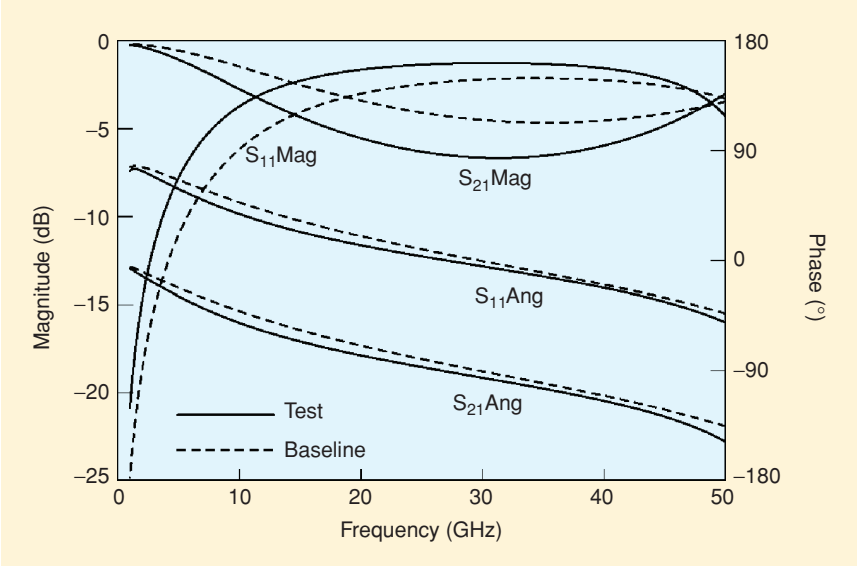

Figure 9. *The test versus baseline (of Figure 6) results when internal port calibration is turned off show substantial differences above about 1 GHz. For this case, it is likely that failure to use internal port calibration will result in design failure.*

of Figure 6. The differences between the test and baseline structures indicate that lack of calibration would most certainly lead to design failure at all but the very lowest frequencies.

If your favorite EM analysis does not have perfect internal port calibration (and prior to GLG calibration, this is true for all EM analyses), all is not lost. After all, there have been lots of results reported in the literature that use internal ports in EM analysis, and they show lots of the usual good agreement with measurement. (Keep in mind that there is a selection effect here; researchers rarely publish bad agreement.)

We played with uncalibrated internal ports to see how one might get good results without calibration. We found at least one case. If you take the 50-μm distance between pairs of internal ports in the above example and decrease it to 10 μm, the difference between test and baseline drops to about one quarter of that shown in Figure 7.

So, with appropriate constraints on internal ports (like keeping the local ground very small), you can still benefit from the new design methodologies (described below) even if you do not have perfect internal port calibration.

Floating Versus Global Ground Reference

Next, an important point I did not mention above. Figure 5 shows a local ground that is connected to the global ground by a via. That via has inductance, but the inductance is exactly removed by the GLG calibration. The net result is that after calibration, all the local ports connected to that local ground are all perfectly referenced to the global ground.

For all of the above analyses, I used a floating ground. To have a floating ground, the via in Figure 5 is removed during GLG calibration (you just select a menu option). This leaves the local ground floating at some unknown potential above global ground. As microwave engineers, we have been trained on data where all ports are always referenced to the same global ground. The first time we see data where some of the ports are referenced to different grounds, it is a completely new and completely mind-blowing experience. (I remember when it happened to me halfway through my immersion!)

So, at least for now, if you value your sanity, do not look directly at *S*-parameters that have multiple ground references. Rather, memorize this one simple rule for using such data: Only make connections between ports that have the same ground reference. Never ever make external connections between ports that use different ground references. As long as you follow this rule, you will be okay.

A subtle aspect of this rule is that if the component you are inserting has coupling to the global ground, you can not use a floating ground. You must select the global ground option for the cocalibrated ports in that case. Here, our inserted components are so far from the global ground that this is no problem.

When using the floating ground option in GLG calibration of cocalibrated ports, every port in the same group has exactly the same ground reference. However, the ground reference in one group (when we have invoked the floating ground option) is different from the ground reference in all other groups. This will take a little getting used to, but as we will see, it opens up an incredible new world.

How Close Is Too Close?

The GLG calibration exactly removes all the self and mutual inductances and capacitances between all the cocalibrated ports in each group. However, if one group of cocalibrated ports gets too close to another group of cocalibrated ports, the fringing field coupling between the groups is not removed. So, how close can we get before it becomes a problem?

To answer this question, we take the above problem with 50-μm lines connecting pairs of cocalibrated ports and shorten the connecting lines in the test structure until we start seeing bad results. So I shortened the connecting lines to 30 μm (each pair of ports is still separated by the original 50 μm). Test and baseline are still visually identical. Down to 20 μm, the same thing

happens—good results. I am trying to get the cocalibrated ports to fail, and they just won't!

Now, down to 10 μm apart, this is less than the width of the lines. It still does not fail. I'm going to get nasty now—2 μm between adjacent pairs of ports. Everything is still perfectly fine; the test and baseline structures give exactly the same answer! Wow!

The reason becomes clear after we think about it. There is mutual capacitance between the output port of one cocalibrated pair and the input port of the next cocalibrated pair. In the last case above, the distance between these two ports is only 2 μm. This mutual capacitance, which is not removed by GLG, increases as the two ports get closer together. But the line connecting them shorts that capacitance out, so it doesn't matter. As long as you have a line connecting them, the floating ground cocalibrated port groups can be as close as you want. There is no problem.

Or is there? Remember, we are trying to break the calibration. Our success above is really just a failure to fail. We failed to fail when using 50×12 μm lines as the component to be inserted. Let's keep the test structure the same, but now insert 50×2 μm lines (Figure 10). Now, the baseline structure is an alternating cascade of 50×2 μm lines and 2×12 μm lines [Figure 10(b)].

For the test structure, the 12- to 2-μm step in width is included in each end of the component to be inserted. There is no coupling between one component and the next.

Do you see what is going to happen? The output of one component has a 2- to 12-μm step. The input of the next component has a 12- to 2-μm step. These components are both included by means of nodal analysis. Thus, any fringing field coupling between the two steps (separated by only 2 μm) is not included in the analysis. This should be substantial. The analysis should fail dramatically. It did not cooperate. Once again, it failed to fail. Test and baseline are almost

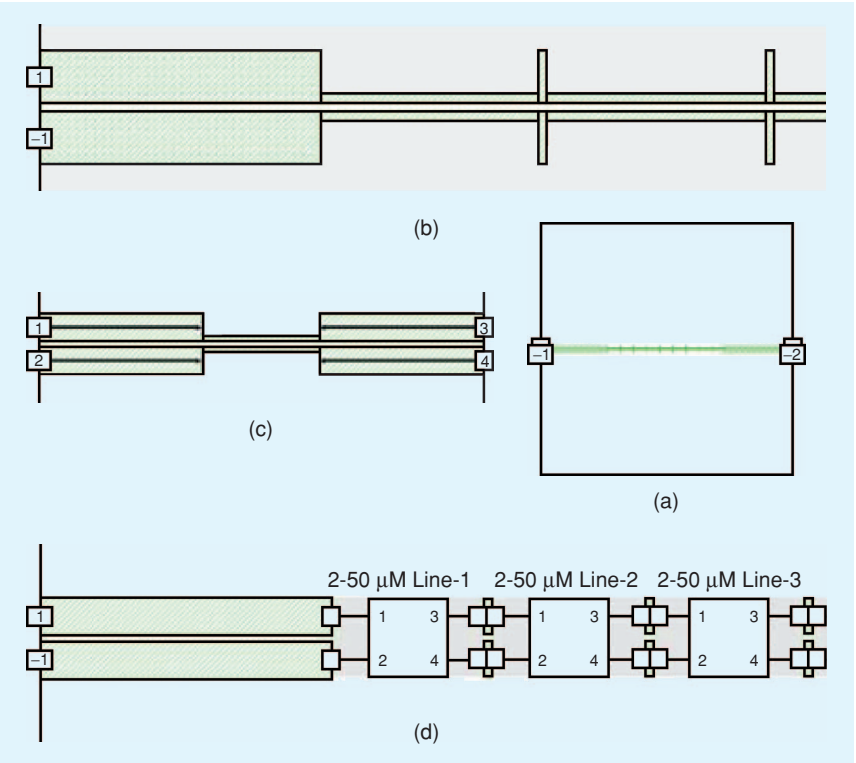

Figure 10. *The cocalibrated ports are grouped into pairs that are 50 μm apart. Here, the groups themselves are separated by only 2 μm. (a) and (b) are the baseline structure. The component (c) is inserted into the test structure (d) and compared to the baseline structure (a), (b). Almost exact agreement is realized as long as the cocalibrated ports use floating ground references. The lines to the left box wall ports have been graphically shortened in (b) and (d).*

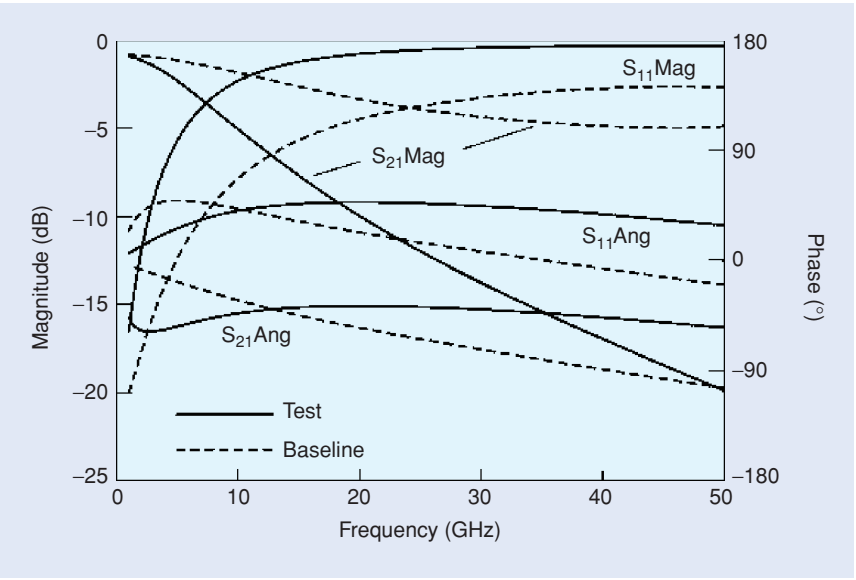

Figure 11. *When the cocalibrated ports are referenced to global ground and one group of ports is close to another group, the GLG calibration fails because of coupling between vias (which provide the global ground reference) in different groups. Fringing field coupling between ports in the same group is exactly removed by the calibration.*

exactly identical; the maximum difference is just barely noticeable when plotted and is under 0.2 dB.

This is astounding. With 30 years experience, I would say Figure 10 shows open-circuited stubs. Attempts to model an open-circuited stub as a close cascade of two large steps in width would be doomed to failure because of fringing field coupling between the steps. However, this is not the case. Instead, at least in this case, it works really well. The creative designer will see some most interesting possibilities.

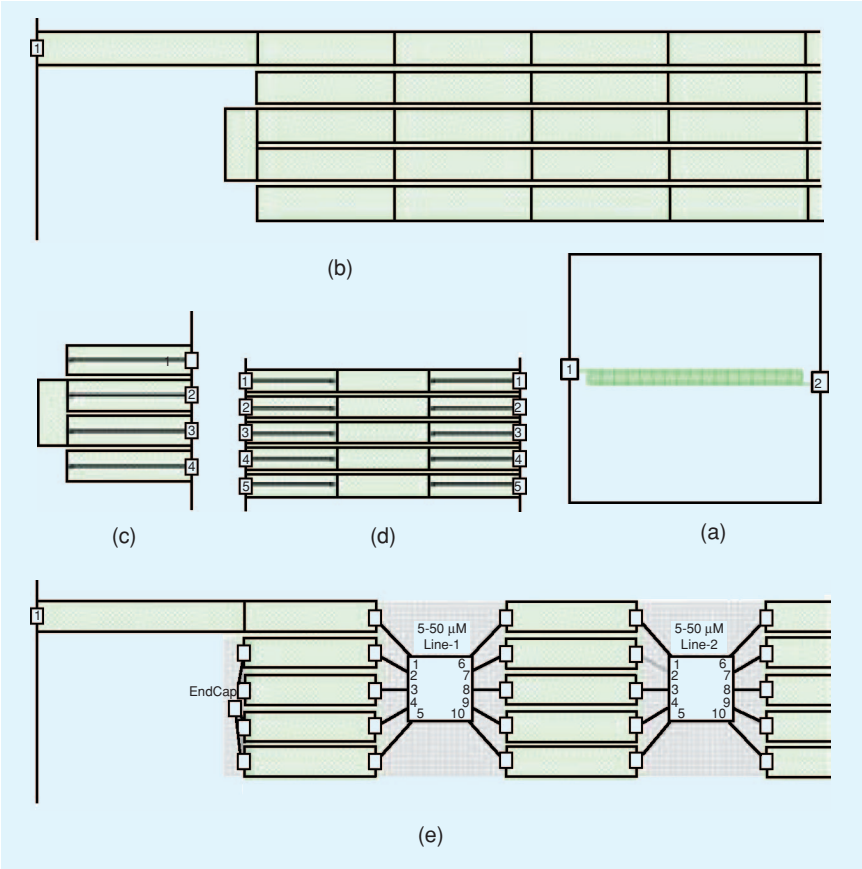

Figure 12. *We can form the S-shaped resonator of the baseline structure by connecting the illustrated component into the test structure.*

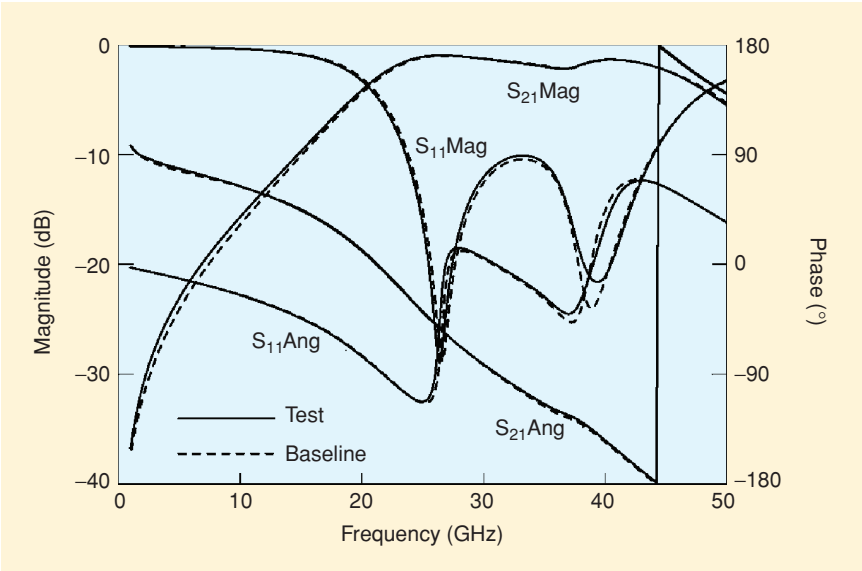

Figure 13. *The response of the S-shaped resonator test structure is nearly identical to the baseline structure. Differences are likely due to the ground return current ambiguity described previously in the text.*

Figure 11 shows what happens when we switch the cocalibrated ports to a global ground reference. Now, the local grounds each have a via to the global ground, as in Figure 5. However, the mutual inductance between vias in different cocalibrated port groups is not removed by the GLG calibration. With the global ground referenced ports of different groups now so close, and the ground connecting vias so long, the calibration fails. Thus, it is a good idea to keep global ground referenced cocalibrated ports some distance from each other. For this circuit, keeping the groups of globally grounded cocalibrated ports 50 μm or more from each other works fine.

Resonator Validation

Our next validation is more complicated and directly suggests the new EM design methodologies. Figure 12 shows the baseline structure of an *S*-shaped resonator. When we insert the indicated 4- and 10-port components into the test structure, we should get the same result as for the baseline structure. And, as shown in Figure 13, we indeed do. Differences that can be seen there are likely due to the ground return current ambiguity discussed above. However, the differences are so small, this would be difficult to test.

Now, we can start to see the new methodology appear. We can put any component we want to in these cocalibrated ports. In Figure 14, we show the exact same test structure, but we insert several different components. Now,

we have a completely different circuit—a cascade of many inductors. (The last inductor is not really an inductor, but this is just for illustration.) The cost of analyzing this new circuit was just the cost of analyzing the new components. The test structure was unchanged, and we reused its analysis directly.

Figure 15 shows the result. Notice that while results are very good, test and baseline results are not quite identical. Recall that fringing field coupling between a component and the rest of the circuit is not included. Notice also that both end components [Figure 14(d) and (e)] are adjacent to the feed lines that connect to the box wall ports. The coupling from the test structure feed line to the immediately adjacent component is left out of the analysis. To test this hypothesis, we simply include that section of the feed line as part of the component. Now the end component is a 6-port rather than a 4-port. When we do this, the only visually discernable difference is about 0.15 dB on S_{11} above 35 GHz. No other differences between test and baseline are discernable.

Thus, lines that are parallel to and very close to a component area should be avoided. For this geometry, there is no problem below 35 GHz for the given geometry: 12 micron long by 2 micron gap between the line and the component. However, if you go above 35 GHz, you should consider either moving any lines that are really close to the component or actually including the line as part of the component.

The New EM Methodology

In its simplest form, the new methodology allows us to remove all active devices from a circuit and substitute perfectly calibrated internal ports. Now we can analyze the entire circuit. We no longer have to analyze the input and output matching networks separately. This allows us to evaluate things like amplifier stability, where coupling between input and output matching networks is critical.

The new methodology does not stop here. Now that we can take out the transistors, why not take out all the capacitors and resistors? You can put cocalibrated ports in their place and analyze all the interconnect of your circuit using EM analysis. For large circuits, the EM analysis is the time-consuming part, taking perhaps overnight or even longer. When complete, quickly connect in the components.

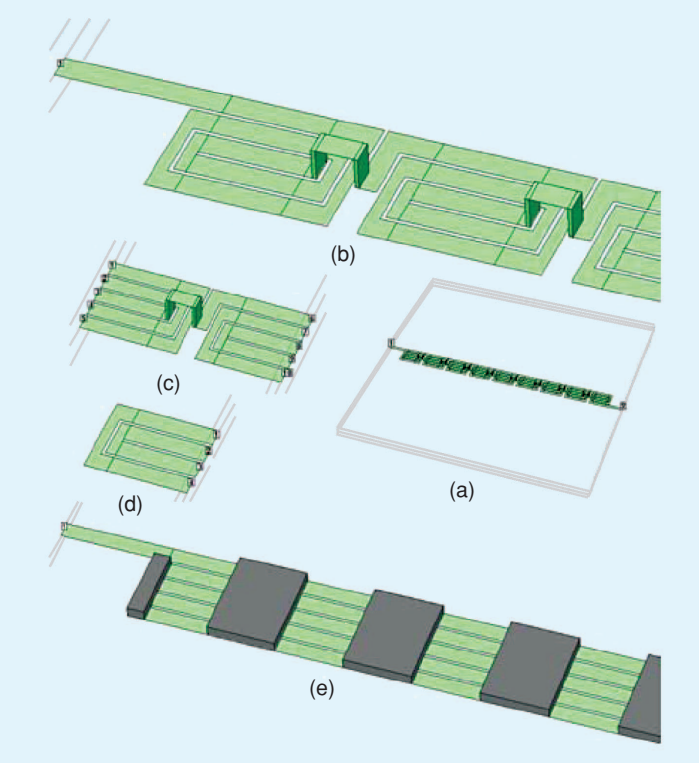

Figure 14. *Using different components for insertion, we can transform the exact same test structure into a completely different circuit, a cascade of spiral inductors (a), (b). The original test structure data is used directly. Only the new components (c), (d) require analysis for this result. They are connected into the test structure (e) in locations indicated by the dark grey boxes.*

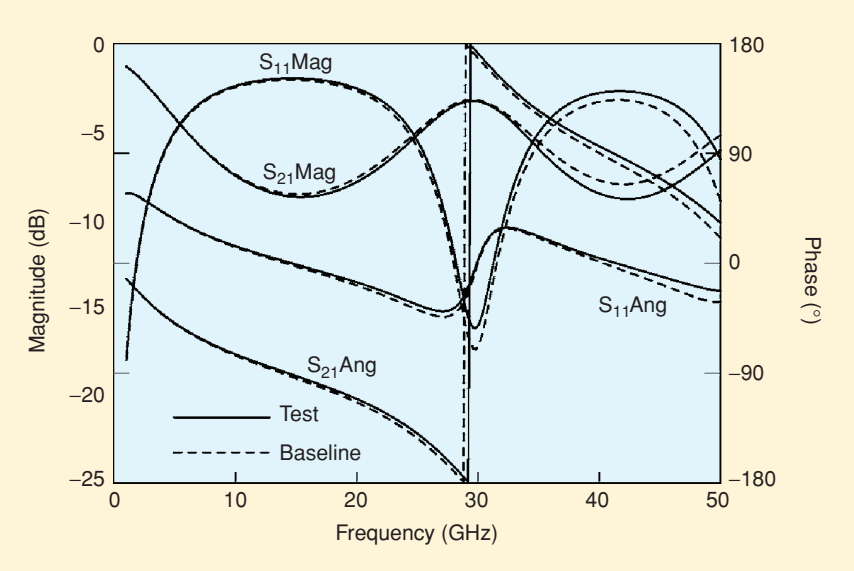

Figure 15. *The response of the cascade of spiral inductors shows a small difference between test and baseline results. The differences are due to the coupling between the end components and the adjacent feed line, which is not included in this analysis.*

This is where the incredible power of this approach appears. After you use circuit theory (either in your favorite framework, or automatically right in the EM analysis) to connect the components, you check to see if your circuit meets requirements. Of course, it can use some improvement. So now, you just change a few of the appropriate components and repeat the circuit theory analysis. You have the new answer faster than you can take a sip of coffee. You can evaluate hundreds of potential designs to full EM accuracy in a single morning.

In the old way of doing things, we would analyze the entire circuit in the EM analysis, come in the next morning and see that the circuit needs some work. So you change the value of one resistor or capacitor and repeat the EM analysis. Then come back in the next morning to view the new result. This is one day per iteration, rather than one sip of coffee per iteration. Simply not competitive.

Notice that I did not include inductors in the component list above. Inductors tend to spread fields over a large area. It might very well be possible to include inductors among the components you remove from the EM analysis, but first check to see how much space you must leave around them in order to get results sufficiently accurate for your needs. How do you check for that? Just like we did above. Analyze a baseline and a test circuit and compare the results. The components you insert into your test circuit will be spiral inductors.

Another application of the component-based methodology is illustrated above in the final two examples—the resonator and the cascade of spiral inductors. Notice that the two very different circuits use exactly the same test circuit. The only difference between them is the components inserted into the cocalibrated ports. This means, with careful consideration of where you place cocalibrated ports, you can now have preanalyzed boiler-plate circuits. When you want a new design, just analyze and insert new components that yield the desired circuit and use the original boiler-plate EM data.

One final area in which the component methodology will have significant impact is in the solution to the "big/small" problem that universally plagues EM analysis. In the big/small problem, we have a large circuit with large structures and large dimensions. Contained in that circuit is a small area that has fine dimensions. Typically, the meshing is set, to some degree, by the small fine structure, slowing the entire analysis of the complete structure. Now, we can just take the small, fine structure region out of the large structure and replace it with cocalibrated ports. The fine structure is then analyzed using very fine meshing. It is then inserted, as a component, into the large structure.

The classic example of the big/small problem is a power amplifier. The matching and bias network is the large structure. The power field-effect transistor (FET) is the small structure. The matching network might have line widths on the order of 10s and 100s of microns, while the FET has line widths on the order of fractions of a micron. The FET is treated as a component. As for the active portion of the FET, one can simply include a set of cocalibrated ports to which you will connect the controlled current sources, one (or more) for each FET finger. In this way, it is possible to build a very sophisticated scalable model of a power FET. This is presently an active topic of my research.

You might notice that some of what I describe above is similar to something popularly and frequently called "cosimulation" from some years back. This is where lumped components could be included in an EM analysis. In reality, of course, they were usually included with what amounted to nodal analysis. In spite of all the marketing promotion and sales presentations, the cosimulation model simply could not work for high-frequency and high-accuracy requirements until the advent of perfectly calibrated internal ports. We now have perfectly calibrated internal ports. A whole new universe beckons.

Conclusions

I have introduced a lot of new concepts in this article: perfectly calibrated box wall ports, perfectly calibrated (cocalibrated) internal ports, floating ground references, global ground references, several new component-based design methodologies, and baseline versus test structure validation. It is going to take a while for our design community to fully understand and explore the impact of these new concepts. I have no doubt that there are some aspects that I have not yet even imagined. The next few years are going to be an amazing time for RF design.

Acknowledgment

The initial baseline versus test structure used for validation in this article was first developed and described to me by Jim Carroll and Tiffany Broome of Raytheon, Dallas.

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