

Advanced Schematic/PCB Design Environment

Pulsonix - Setting the new standard in PCB layout

Pulsonix is a PCB design & layout suite of tools developed to meet the changing needs for PCB layout in the 21st century.

The first completely new, high level combined Schematics Capture & PCB layout product for many years, this exciting software tool has been developed from the ground up by PCB Design industry professionals using the very latest techniques in graphics and data handling.

Pulsonix has been designed based on key criteria:

- Easy to use by way of an intuitive user interface
- Designed for the casual user and the professional
- Imports design and library data from key EDA products

Easy to learn and logical to use

Pulsonix has been developed with an easy to understand user interface using Microsoft standards, look and feel.

The menu structure is logical and intuitive moving from left to right as you progress through your design process. The toolbars and keyboard keys are fully configurable so that at all times you have shortcut keys and tools to hand, making the design process more efficient.

Training needs kept to a minimum

A key principle in the design of Pulsonix was to create a product where the need for structured user training could be minimised. This has been implemented and you will find that you are productive with Pulsonix in a very short time. Pulsonix is delivered with an informative Users Guide and up to date, context sensitive on-line HTML help.

Designed with the future in mind

Pulsonix is built on the latest concepts in software design, hence it has many years of development life and expansion ahead.

With the need for constant growth of a product through customer feedback and market demands, Pulsonix is well positioned to grow with any technology or trends that are being developed, and even some that are years ahead!



Directly Imports Schematic & PCB Designs and Libraries from:

OrCAD Capture / Layout PADS PowerPCB/Logic/PowerView Accel EDA Cadstar For Windows Altium Protel 98/99SE P-CAD MasterDesigner/2000-2006 UltiBoard and UltiCap Eagle Cadence Allegro Integra Mentor DxDesigner/Viewlogic Visula Zuken System Designer EDIF

Schematics Electrical Rules Checking (ERC)

On-line and batch checking setup using a table of ERC rules in Technology Includes user definable rules.

User Definable ERC Rules

<Undefined> <Undefined> {Block Port} **Bi-Directional** Ground Input Input (Block Port) Open Collector Open Emitter Or-Tieable Output Output (Block Port) Passive Power Terminato Tri-State

Name

XB Output

B Or-Tieable

B Terminator

B Open Emitter

B No Connect

B Tri-State

B Power

B Ground

B Passive

XB Input

Pin types can be user defined then selected in the component library definition. XB Bi-Directional Permutations of bin B Open Collector type connections may then be selected in the Electrical Rules Checker to determine Error or Warning situations when adding connections to the design.

Bi-Directiona

Doen Collecto

. Open Emitte

nput (Block Port)

iround

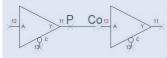
Output Dutput (Block Port)

assive

ower

erminato

Tri-State



You can easily zoom straight to an ERC error. In this case 'P' denotes a single pin net error on the output and 'Co' a connection error, as the connection between components is broken.

Auto-Dim

This powerful option enables items which are not selected during editing to be 'dimmed' or low lighted so they become unobtrusive while editing the area of concern. This is especially useful when editing large multi-layer designs, which can be very confusing due to the volume of items being presented in the design window at any one time.



Fully supported on 32 & 64 bit operating systems:

Windows® Vista, Win 7 & 8

Easy to learn and use

Designed to be extremely easy to learn and use for both the casual user and PCB layout professional. New customers usually pick-up Pulsonix within a day or so of use

Flat Sheet and Multi-level **Hierarchical Design**

Pulsonix provides 'top down' design: breaking blocks into functional elements allowing you to define the detail of each element, and bottom-up' design: facilitating the re-use of commonly used circuit elements using pre-defined blocks to build a solution.

Constraint-based Rules

Net Class rules can be defined in the Schematic design and automatically passed through to the PCB design editor. This means rule definitions are set further forward in the design process.

Windows Drag & Drop

Easy, pick, drag and drop operation, no additional 'modes' to click or enter before being able to move items.

ERC/DRC Error Viewer

ORC Errors	×
- DRC errors: 64	_
 Board to Text Error (B-X) 	
E Layer: 1-Top	
Between (-4954.0 -3250.0) and (-4954.0 -3215	5.0)
Layer: 2-Ground	
Layer: 3-Power	
Layer: 4-Bottom	
Component to Component Error (Cm-Cm)	
 Pad to Pad Error (P-P) 	
Pad to Track Error (P-T)	
 Pad to Via Error (P-V) 	
 Track to Track Error (T-T) 	
 Track to Via Error (T-V) 	

Where design rule errors are produced, a browser displays the errors by layer and type for easy identification. By selecting the marker from the list, the design area moves to the element in error.

Schematic Symbol Wizard

Takes you through creation of the symbol in a step-by-step sequence to easily produce regular symbols. The pin sizes, positions and numbering is selected to make symbol creation so simple and error free.

Workbook Mode

The Workbook tabs allow you to quickly identify open designs and libraries by name. Clicking on the tabs enables quick switching between any open window.

Active Status Bar

Gives you an instant Property status on any selected item in the design without the need to use a Query or Properties dialog. Using a double-click on the Status Bar provides you with instant access to Grids and Units.

Modal Cursors

With the modal cursor option on, you are given an indication of any available modes by a symbol appearing with the cursor. This provides you with instant feedback of the option available during key operations.

Import/Export DXF and IDF **Data Formats**

Import and Export of both DXF and IDF formats are available, this enables you to communicate intelligently with your mechanical CAD system.

Import Bitmap

Bitmap images may be imported into your designs. These may be your company logo or other bitmaps and symbols required to annotate the design. The design can also be exported to bitmap and WMF formats for documentation burboses.

Fully Customisable Toolbars and Shortcut keys

Using standard Windows technology, you may relocate icons from one toolbar to another. New icons with tools of your choice may be added to the toolbars. All existing shortcut keys may be changed and new ones added at will.

Intuitive Graphical User Interface

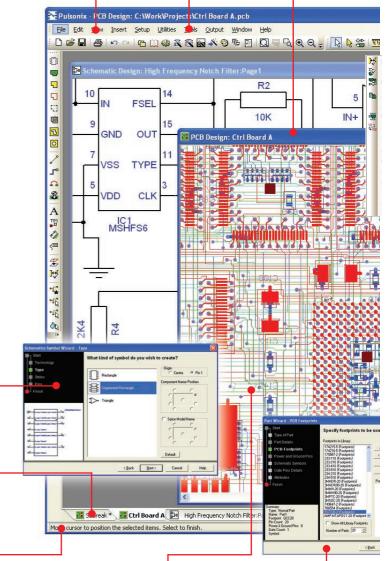
Pulsonix has an immediately familiar feel similar to that of your existing Office products. This means you'll be productive in a much shorter space of time.

Windows Style Interface

Similar to Microsoft Office applications, you immediately know where to find common Windows menu items.

Cross-Probing between the Schematic and PCB design editors

Instant selection of parts & connections in Schematics with the highlighting of corresponding tracks and footprints in PCB and vice-versa.



Component Pushing Mode

An outstanding feature of Pulsonix is the placement 'push' mode. This enables Component placement by 'pushing' other Components out of the way as it is dragged.

Design/Part Variants

Using the Variant Manager, any number of variants may be defined at either the Schematic or the PCB design stage. If using the Schematic as the master, the variant information will be automatically transferred to the PCB design. Detailed part variants can be easily created. Pulsonix allows Fitted/Not Fitted, different Part, Footprint, Attributes/Values, and even a different number of footprint pins per Component.

Part Creation Wizard

The Part Wizard is used to create all kinds of barts within Pulsonix. This useful tool takes you through the process of part creation step-by-step, thereby avoiding the potential for any errors and automating this brocess.

Reverse Engineering Features

Where a PCB design exists in some form but the Schematic doesn't use the Reverse Engineer feature to rebuild the Schematic from the PCB. Either, intelligently import a PCB Gerber file and using part-based symbols, rebuild the design to the Component Bin ready for placement, or trace over an imported bitmap. These features will save you many hours of work.

Single-Shot Postprocessing

Manufacturing output is simplicity itself with the latest in technology single-shot post design processing. Just set up the plotting parameters once and from then on it's a single click to produce all your plots. Pulsonix produces professional results using standard manufacturing outputs.

Synchronise Designs

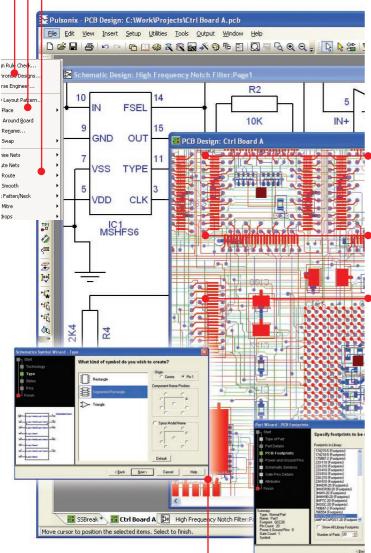
Provides an instant report of differences between the Schematic and PCB designs to check design integrity. Automatic updating to the PCB is run on completion of the operation. Component and Net renames are back annotated to the Schematic.

Integrated Automatic Placement

Initial automatic blacement is driven through a single dialog with no previous set up required. Placement rules driven off this dialog make the option easy to use. Placement can be made to/from groups, around the board outline and using named areas

Gate & Pin Swapping

Manual and Automatic Gate & Pin Swapping is provided to assist placement and optimise the overall connection lengths. Interactive displays of swappable gate sets show the source and target gates for swapping. This information is easily created in the Parts library for reuse on each design.



Pad IC16.93 on net PerData6 Width: 1.854 Height: 0.604 Laver: <Top Side PadJC1519 Width: 0.604 Height: 1.854 Laver: <Top Side Layer: <Top Side Distance Shortest Gap Dist: 10.262 X: -9.299 Y: 4.340 Angle: 205.0 Spacing: 0.150 Units: mm I Snap t Hide Report...

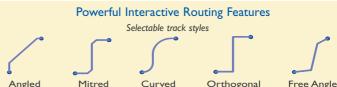
An interactive option to measure the gap between any two design items. Select the first item, then a target item, the Measure tool dialog displays the distance between the two items. This is the real distance between the points as would be calculated through the DRC option and is measured against the closest point of each item selected. Other useful information about the selected items is also disblayed.

Measure Tool

Footprint Wizard

The easy to use Footprint Wizard breaks down the process of creating a new footprint into a series of logical steps. It enables auto-production of DIP, SOIC, PGA, BGA, Quad and Radial devices using a clear graphical user interface.





In the knowledge that the layout engineer usually devotes a great deal of effort on interactive editing, Pulsonix has been designed to be a pleasure to use. Extensive use of context sensitive, right hand mouse menus gives you instant control on track types, styles, layers and grids.

Design Browser



The design browser provides design management of all open designs and blocks.

World View

Gives a complete display of the view showing the area of zoom. This window can be used interactively with the mouse for precise zoom selection.

Component Preview

Displays selected components from the Component Bin to ensure selection errors are not made.

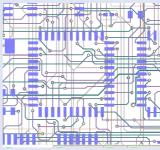
Component Bin

Provides a convenient 'off-design' location for Schematic and PCB Components during the design process.



Pulsonix is a registered member of the Valour partner program and exports manufacturing data in ODB++ format. This is fast emerging as the defacto standard for PCB CAD manufacturing output and is accepted by most leading manufacturers.

Integrated Pulsonix Autorouter



Report Generation

As well as an extensive set of design reports supplied for use during the design process, a powerful user definable Report Maker option is also available. This highly configurable option allows you to output all entities of the design in your own customisable format.



If the track is placed closer to the obstacle the colour

is given of the nearest be placed passing an changes to red. showing a violation.

On-line Design Rule Checking

Real-time spacing rules checking with instant feedback of warnings before the error occurs. 'On-Line DRC' may be set to completely prevent errors occuring during the edit process.

Extensive Batch DRC

point the track may

unconnected bad.

Extensive Design Rules Checking means that all aspects of the design can be checked. This rule set includes spacing rules, on/off grid items, keep-in/out items, single pin nets, unconnected pins, plus manufacturability checks of the design.

Spacing	P On Grid	Mani	Aschuring		Nets
7 Tracks	Tracks	T Isola	ted Copper	Г	Single Pin Nets
Vias	Viss	I Unpo	ured Templates	Г	Net Connectivity
Pads	Test Points	I Une	achable Testpoints		Unfinished Track
Mount Holes	Components	Minimum Probe Points			Track Layer
Test Points	Pade Pade	V Split	Plane Pad	Track Width	
Copper		Plane Themal Pad		Via Size	
7 Test	r Keep In/Dut	Gond Wire Length		Track Length	
Board	Tracks	Wire Cross		Connection Length	
Dillo	Via:	Wire Under Component		Connection Vias	
Components	✓ Test Points	I Dril Backoff		Pin Order	
SpR Planes	Components	Minimum Pad Land		Dillerential Pairs	
	Copper	Pad Undersize			
	🔽 Drils	Com	conent Name		
	S	lié toele	Deselect All		
Acceptance Rule	Set - Enor Marke	15	Output		Source
Load		Looked 🔽 Generate Re		int	Design
7080	Enor		Report Ru		C Selection
Save Clear All		Errors	1018 Not Checked		C Window
		_			WEIGOW

STEP Mechanical Interface

Where a mechanical interface is required, you can use the STEP interface to bi-directionally use models and import critical board outlines and positional changes. The STEP exporter will write the board outline out ready to add mechanical data. The built-in STEP previewer allows you to examine and verify the design data before you send it to the MCAD system.

- Integrated into Pulsonix PCB
- Supports single-sided, double-sided and multilayer boards
- 45 degree routing algorithm
- Shape-based gridless routing
- Post-routing optimisation passes
- Fanout pass for breakouts
- Routes SMDs on both sides of the board
- Supports blind/buried vias
- Full and split Plane/Ground Planes support
- Route by Net/Net Class
- Ability to fix critical pre-routing
- Uses spacing rules by design/net class/net
- Via rules by design/net class/net



FEATURE OVERVIEW

General Features

- Supported under Windows XP,Vista, Win 7 & 8
- Ultra-fast bitmap graphics
- Database resolution to 1/100th micron
- Object Oriented Mosaic[™] Architecture
- Connective data structure (not net-list driven)
- Rotation to 1/1000th degree
- Active-X Scripting language support
- Internal Macros supported
- Standard interface for integrated SCM/PCB
- Fully integrated design environment
- Component Bin with preview
- World View of design
- Customisable Toolbars/Shortcuts
- Dockable and Floating Toolbars
- Technology files for fast start-up
- Comprehensive Parts library
- Integrated library editors
- Dynamic Pan, Zoom In/out
- Right mouse shortcut menus
- Drag and Drop methodology
- Intelligent copy, paste & duplicate
- Output to bitmap for documentation
- Update/edit Parts on-the-fly
- Multi-level Undo and Redo
- Transient and Persistant Groups
- Full and flexible user-defined report generation
- Star/Delta point support for multiple signals
- Support for FPGA devices built-in as standard
- Comprehensive item property reporting
- Design & Part Assembly Variants
- Item Align function
- Support for Windows graphics driver library
- Floating Network Licensing available
- Import Schematic, PCB Design and library data from many other systems

Schematic Capture

- Design in mixed Imperial or Metric units
- True connectivity during all operations
- Fully customisable interface
- Save and Load Technology files
- Symbol creation wizard
- Scaled Symbols
- Graphical Symbol and Part editors
- Support for multi-gate logic and irregular devices, such as relays
- Save and Load Drawing profiles
- Uses common Parts libraries with PCB editor for smooth transition from SCM to PCB
- Flat sheet or Multi-level hierarchy
- Single or multi-instance of the design block
- Automatic security copy and backup of designs
- Intelligent Open and Closed Busses
- Reuse of designs using blocks or copy/paste
- Dynamic drag & drop move, rotate and mirror Parts or groups
- Autoweld functions
- Predefined and user defined attribute fields for custom title blocks and auto-updated detail

20 Miller Court, Severn Drive, Tewkesbury, Glos, GL20 8DN. UK Tel: +44 (0)1684 296 551 Fax: +44 (0)1684 296 515 E-mail: sales@pulsonix.com Web-site: www.pulsonix.com

- Automatic/manual Component & Net rename
 - Electrical Design Rules checking including: preset and user definable rules design integrity rules

Integrated Copper Pour with Hatching

Gerber Photo-plotter to RS-274-D and

RS-274-X (extended aperture format)

Automatic generation of power-plane plots

Automatic Gate and Pin Swapping

Change Components on-the-fly

Supports true split Power-planes

Built-in PDF driver for active PDF files

Excellon NC Drill output and drill drawings

Mechanical Design Input/Outputs in STEP, DXF

 Import Schematic Netlists using: EDIF 2.0.0, OrCAD, Viewdraw, EWB and other vendors

Plotting of solder masks, resist and other

Dynamic Dimensioning

ODB++ Format exporter

IPC 356 test format output

Output to GENCad format

Windows printer outputs

Plotting to HPGL plotters

manufacturing plots

and IDF formats

Integrated LPKF Interface

Cost Option Features:

Advanced Autorouter

Bus routing

Micro-via support

and spiral inductors

Chip-on-board design

- Die and Bond pad support

Uses an adaptive routing strategy

Constaint rules spreadsheet

Advanced Technology Suite

Embedded component technology

Interactive High Speed Routing

Constraints driven net length management

Edge & Broadside couple differential pairs

- Stacked, tapered and lasered Micro-vias

- Component placement into cavities

- Component placement on flexi layers

- Flexi-rigid design with layer spans

- Independently floating Bond pads

- Rules driven Bond Wire support

Min/Max bond wire length rules

Uses industry standard models

date Part information

2048Mb RAM or higher

PLM product interface toolkit

Pentium Processor 2.0 Ghz or faster

I.6Gb free space on hard drive

- Report and machine driven outputs

- Insulated and Cross-over rules for bond wires

Fully integrated into Pulsonix design environment

Powerful and flexible commerical grade simulator

Connect to your corporate database for up-to-

Product Lifecycle Management (PLM) Interface

Suggested Hardware and Operating System

Microsoft Windows 7 or Windows 8 recommended

PSX110913

Spice Based A/D Mixed Mode Simulator

Pulsonix Database Connection (PDC)

- Buried semi-conductors, thinned dies, printed

resistors, buried capacitors, planar transformers

Graphical length feature and head-up display

Design Calculators

- On-line Electrical Rules Checking (ERC)
- Electrical rules error browser
- Design browser showing all sheet levels including hierarchical blocks
- Constraint rules definition passed through to PCB design editor
- Save and Load Colour files
- Truetype fonts support for display and printing
- Cross sheet references
- Power and ground labels
- Testpoint Part and notation insertion
- Back annotation of design changes to/from SCM
- Synchronise design at any time to check design integrity between SCM and PCB designs
- Back annotate all changes from PCB
- Windows and pen plotter outputs
- DXF Import and Export
- Export Netlists
- User definable Parts and Netlist output

PCB Layout

- Design area up to 10.0m by 10.0m (393" by 393")
- Design in mixed Imperial or Metric units
- Relative and Absolute coordinate system
- Unlimited number of user defined layers
- Supports SMT, through-hole, mixed & slotted-hole technologies
- SMDs on all sides of the board
- Blind and buried via support
- Via stitching into/around areas and tracks
- Advanced Footprint Rules Technology
- Dynamic drag and drop
- Wizards for: Data Transfer, Footprint creation & Parts creation
- Track/Via breakout/fanout on footprints
- Wire and jumper support in design & parts
- Manual Placement 'push' and 'return' mode
- Integrated Autorouter and Autoplace
 Design item Keep in/out areas
- Design item Keep in/out areas
 On-line and Batch Design Rules Checking
- On-line and Batch Design Rules Checking (DRC)
- On-line Display Clearances
- Design rules error browser
- Spacing shapes to add clearance to pads/vias
- View your boards using the built-in 3D Viewer

Single track Autorouter

Dynamic Net Optimisation

User definable Report Writer

Copyright @WestDev Ltd 2013. All rights reserved. E&OE. Pulsonix is a registered Trademark of WestDev Ltd. All other trademarks are acknowledged to their rightful owners

Teardrop insertion on pads and vias

Net Find, Highlight and Select browser

Construction lines

n.

n.

- Manual Routing angle modes Free angled, 45 degree, Orthogonal and Curved
- Manual Routing modes: Pull-tight, Track pushing, Auto Corner, Auto Mitre

Automatic Net Testability and Testpoint Analysis

Reverse Engineer, rebuild SCM design from PCB

Many Report outputs including Parts list & BOM

Rebuild Gerber files intelligently into design format